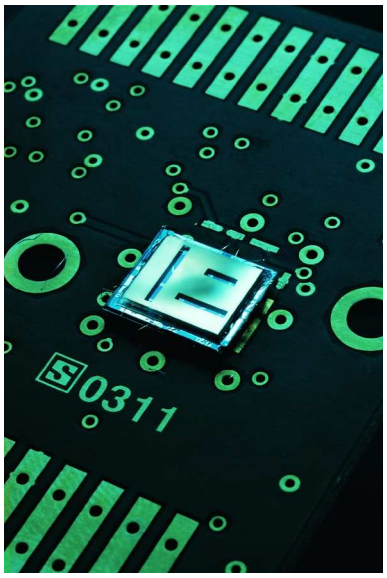
Linear Two-Axis MOEMS Sun Sensor

Part of the DTUsat project – and beyond



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Technical Report

MIC – Department of Micro and Nanotechnology
Technical University of Denmark (DTU)

Supervisor: René W. Fléron

24th August 2004

MEMS In Space @ MIC

From left: René W. Fléron, Jan. H. Hales,
Martin Pedersen, Anders Torp, and Philip R. Bidstrup.

The DTUsat presented is an early engineering model.

Abstract

This report describes the work conducted through the design, development, fabrication, testing, and integration of a sun sensor system initially designed for DTUsat – a Danish student CubeSat project at the Technical University of Denmark. The main focus of the report will be on the developed Micro Opto Electro Mechanical System (MOEMS) sun sensor device. The sensor chip is $\sim 7 \times 8\text{mm}^2$ with a Field of View (FOV) of $\pm 70^\circ$ and a resolution better than 1° is obtainable for -40° to 40°; beyond these angles a resolution below 1° is more difficult to obtain.

Device principle and design are thoroughly described to give a clear understanding of the considerations made along with a justification of the various design choices. For comparison other existing MEMS sun sensors are also briefly described. The microfabrication processes are treated in depth both to give an insight to the various procedures, but also to suggest possible optimisation approaches. Additional performance results such as an initial quantum measurement and IV characteristics are presented and analysed.

This report is mainly written for engineering students who would like to continue the work on the sun sensor. The report gives a detailed overview of the project. Many technical details have naturally been left out to keep the length of the report down. More detailed documentation and measurements are available upon request.

Preface

This project was carried out at the Department of Micro and Nanotechnology (MIC) at the Technical University of Denmark (DTU).

The report at hand is written as part of a 15ECTS points (for each student) special course, and it describes a MOEMS sun sensor that was initially designed for DTUsat. The project also involved a lot of practical work which is also included in the evaluation of the project.

The project was supervised by René W. Fléron who initially was employed as a process specialist at MIC, but is currently in the same function at DANCHIP, DTU. We would like to thank René W. Fléron for his great help and extreme enthusiasm during the two years the project has lasted!

Associate Prof. Ole Hansen (MIC) is acknowledged for his insight and ideas within semiconductor technology. Prof. Mogens Blanke (Ørsted•DTU) is thanked for his dedicated involvement on DTUsat, and Assistant Prof. Mike van der Poel (Research Center COM) is thanked for providing equipment and guidance for the optical setup.

Our partner in the ACDS group on DTUsat, M.Sc. Student Klaus Krogsgaard who developed the magnetometer, is thanked for his great knowledge within electronics design, and for the many enjoyable hours we spend in the lab together.

The staff at MIC are also acknowledged for their various expert opinions and design reviews, and the entire DTUsat group and especially the system engineering group is acknowledged for its project coordination and management.

Finally we would like to thank the wide range of sponsors and foundations who not only contributed to this specific system, but also made it possible to construct and launch DTUsat.

Martin Pedersen

Jan H. Hales

Kgs. Lyngby, 24th of August, 2004

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1

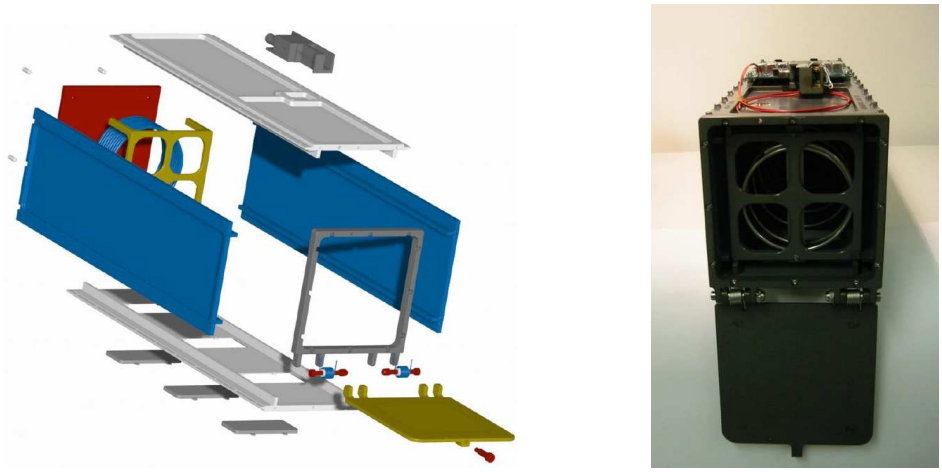
Introduction

In the summer of 2001 a group of students at the Technical University of Denmark (DTU) teamed up with the idea of building and launching a satellite in just one year! This very ambitious goal – none of the students had any experience with satellite construction – was made to keep the motivation going during the entire project. It was thought that the students would be less enthusiastic if their project would not be launched while they were still students. However, after the initial design phase the suggested satellite was too complex to be realised in just one year. Instead of making a simple and "boring" satellite the students decided to extend the project to two years – the DTUsat project was born.

It was chosen to construct DTUsat as a CubeSat, which is a precisely defined external structure of $10\times10\times10\text{cm}^3$ and a mass of maximum 1kg [39]. The CubeSat structure was proposed and initiated by Professor Bob Twiggs, Stanford University and Professor Jordi Puig-Suari, California Polytechnic State University (Cal Poly) in 1999 as an easy and cheap way of launching pico satellites[1]. The low launch costs of 35,000-70,000USD per satellite is achieved by integrating CubeSats in a Poly Picosatellite Orbital Deployer (P-POD) which basically is a tube that can hold three CubeSats and deploy them once in orbit – see figure 1.1. The P-POD lowers the costs since it allows simple integration of CubeSats in launch vehicles that have one or more P-POD(s). The simplicity of the P-POD and the low mass makes the CubeSats ideal for tertiary payloads (piggybags) which of course also plays a central role for the low costs.

The CubeSat structure was chosen to allow cheap *and* easy access to an orbit after final construction. However, this proved a bit more troublesome than we had expected since no CubeSats had been launched and nobody was using P-PODs! So finding a launch provider for our CubeSat ended up being a very difficult task which was only accomplished due the great

[1] Pico satellites: class of satellites with a mass in the 0.1-1kg range.



(a) (b)

Figure 1.1: The P-POD (Mk I) *(a)* exploded view, and *(b)* picture. The P-POD is also available in a twin version with the capacity of six CubeSats.

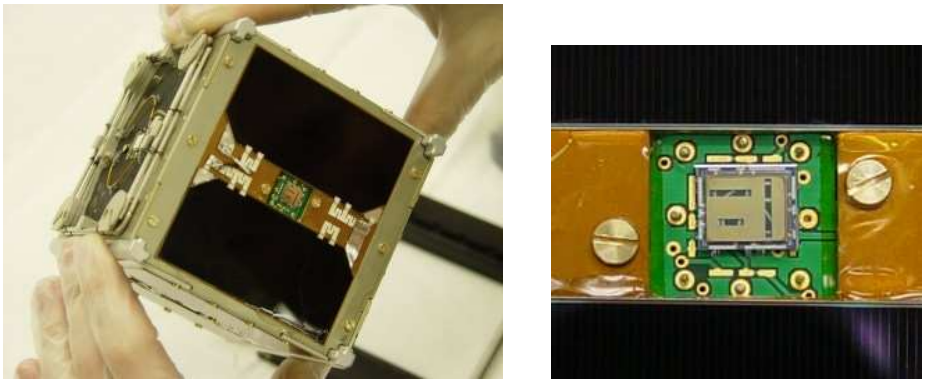
assistance provided by the Danish Space Research Institute (DSRI). DTUsat was on the very first launch of CubeSats ever, whereas the earliest groups that started out in 1999 still have not launched their CubeSats!

The authors of this report and M.Sc. Student K. Krogsgaard carried out the overall design of the Attitude Control and Determination System (ACDS) of DTUsat as their B.Sc. thesis project [14]. In this project it was e.g. determined that the ACDS hardware should be magnetotorquers for actuating and magnetometer & sun sensors for attitude determination. Both sensors are needed for unambiguous attitude determination since magnetometer and sun sensors do not tell you how you are rotated around the magnetic field lines and the solar vector respectively. A general design was made of both sensors, but the detailed design was later divided into two large projects – a magnetometer part carried out by K. Krogsgaard [24, 23] and a sun sensor part described in this report.

1.1 An Overview of DTUsat

A group of approximately seventy students have been involved with the DTUsat project and about fifteen students have been fully involved during the entire project.[2] A picture of the flight model of DTUsat that is currently in orbit can be found in figure 1.2(a). Figure 1.2(b) shows a close-up of the sun sensor which is the subject of this report.

[2]Official DTUsat web page http://www.dtusat.dtu.dk/.



(a) (b)

Figure 1.2: *(a)* A fully assembled DTUsat before flight to Canada where it was integrated in the P-POD with AAU CubeSat from Aalborg University, Denmark and CanX-1 from Toronto University, Canada. *(b)* Close-up of a sun sensor.

1.1.1 The Purpose of DTUsat – its Payloads

Many instances saw the completion and success of a project of DTUsat's magnitude just as likely as if Sisyphus would ever accomplish the task of placing a huge stone on the rounded top of Acrocorinthus. For the students it was also clear that building a satellite from scratch, launching it, and operating it within just two years is an extremely difficult task considering that none of the students had ever been involved in space projects before! Therefore a prioritised list of goals was made for the project. These criteria of success was used to convince foundations that investments in DTUsat is an investment that will produce better engineers now as well as in the future. An abbreviated version of this list is:

1. Educating the participating students in the topic *space*.
2. Completing the basic sub-systems of a CubeSat and documenting them so that they also can be used on future DTUsats.
3. Giving the students hands-on experience with management and organisation of large projects.
4. Constructing and testing a complete CubeSat on ground – giving birth to the very first DTUsat. This is a large-scale integration project – a topic that has never been taught at DTU.
5. Launching DTUsat into orbit.
6. Establishing radio contact.
7. The criteria of success for professional satellite projects follows here.

That a satellite project produce high quality engineers is a known fact from satellite projects around the world. The engineers, or in our case the stu-

(a)

(b)

Figure 1.3: *(a)* Picture of DTUsat's payload side. The circular hole is the camera window, and the tether coil (shown on inset) is ejected from the satellite when the rectangular door is opened. *(b)* The antenna side of DTUsat. The inset shows one of the springs that is located on each antenna arm to enable deployment.

dents, must combine many different fields, establish interfaces to allow parallel development, and have continual reviews off all ongoing tasks to ensure that everything/everybody is on the correct path. This is naturally tasks that set great demands on collaboration, management, and organisation – an area in which graduating engineering students most often do not have any experience. The requirements to the team and review work are even higher for satellite projects than for normal Earth based projects since first time success is very important in space.

The way the education of good engineers could be continued after the first DTUsat is by recycling the knowledge obtained in the project and passing it on to the next generation. This has in the case of DTUsat been carried out through documentation and lectures given by students in courses on satellite construction. The success of DTUsat is discussed in section 1.1.4.

In addition to the stated goals the ambitious students naturally included science instruments as payloads in addition to the required sub-systems – as on a real science mission. The two payloads on DTUsat are a camera and an electrodynamic tether:

Camera Payload is the public relations payload. Its original purpose was to produce pictures of Denmark, but since the camera electronics was not finished in time only a one pixel infrared camera is present. This can be used to investigate the temperatures the CCD will be exposed to with the developed lens. The CCD camera could of course also have been used for some simple Earth observation applications.

Tether Payload is the real scientific mission on DTUsat. After 1-2 months in orbit a 500m aluminium tether is to be deployed to demonstrate lowering of the orbit due to interaction with the geomagnetic field. The intention is to emit electrons with a MEMS emitter so that we have a current which is closed in a loop in the surrounding plasma [9]. This will cause an resulting Lorentz force on the tether which is then used to lower the orbit. However this is not possible since the emitter was not finished in time – so lowering will only be due to drag. A practical application could be to de-orbit a spacecraft into the atmosphere and burn after ended operation.

1.1.2 The Sub-Systems

DTUsat carries the same sub-systems as a professional satellite. However, since DTUsat is one of the first pico satellites smaller systems than the commercially available are needed. Therefore a substantial part of the DTUsat project has been within miniaturisation.

Figure 1.4 shows how the different sub-systems is integrated in the satellite frame which was milled from one block of aluminium to obtain a rigid structure. The structure is closed with six side panels. Four of these contain solar panels as shown in figure 1.2(a), and the last two contains the payload-space interface and the antenna structure as shown in figure 1.3. All panels except the payload panel contains a sun sensor – the sun sensor here was left out due to lack of surface area. In short the sub-systems of DTUsat are:

Power which utilises solar panels on four sides and is capable of delivering approximately 1.5W. The battery provides additional power during radio transmission where the power consumption exceeds the available solar energy. Latch-up protection is also included in this sub system.

Figure 1.4: Picture of DTUsat during assembly. Bottom PCB: on-board computer (OBC) which serves as a motherboard. Lower side PCB: Radio. Left side PCB: Power. Upper side PCB: Payload. Right side PCB: Attitude Control & Determination System (ACDS). A sun sensor is included on each side panel except on the payload side. The two metal cases are housings for the two payloads: a camera (left) and an electrodynamic tether (right).

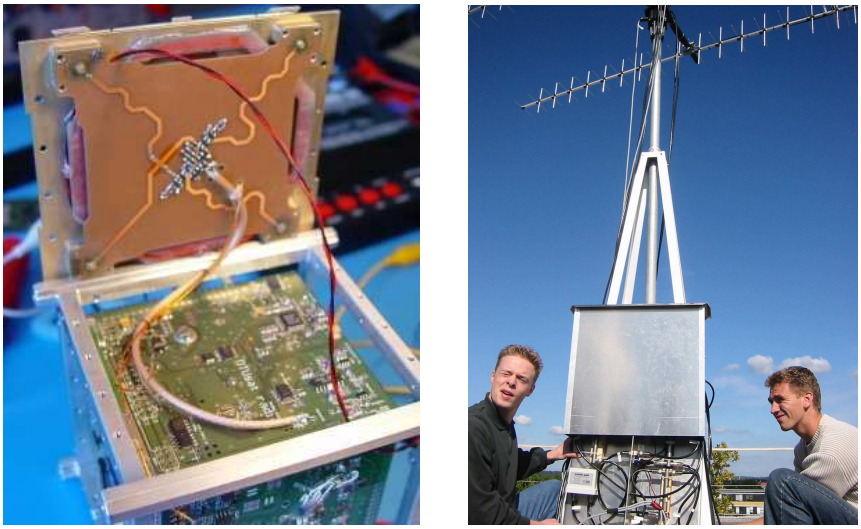
On-Board Computer (OBC) contains of course CPU, ROM, RAM, Flash-RAM etc. Furthermore OBC serves as a motherboard on DTUsat since all PCBs (except sun sensors and camera) are mounted on the OBC.

Radio communicates at 2400bps in agreement with AMSAT with the ground station at 437.475MHz. The antenna is circular polarised and sufficiently omnidirectional to operate without attitude control.

Attitude Control & Determination System (ACDS). The main PCB contains a 4-axis magnetometer, driver circuits for the three 1μNm PWM magnetotorquers which are mounted on the inside of three side panels (see figure 1.5(a)), and a communication port and harness connections for the sun sensors.

As mentioned above all systems except the camera and sun sensors are mounted directly on the OBC. The camera is a stand-alone component since the housing contains both camera, needed electronics, and interfaces. The sun sensors are mounted on the backside of a PCB and bolted to the backside of the panels – detailed information is given in chapter 5.

In addition to the electrical systems DTUsat naturally involved a lot of software coding, mechanical and thermal considerations, and of course a ground station – see figure 1.5(b).



(a) (b)

Figure 1.5: *(a)* DTUsat with open antenna side. The inside of the panel contains feeding network, one magnetotorquer, and a sun sensor PCB behind the feeding network. *(b)* DTUsats ground station antenna (located on top of building 348 at DTU) which can rotate around two axes to enable tracking of DTUsat upon passes.

1.1.3 Organisation

Throughout the project the organisation has been one of the most challenging problems. The individual sub-system groups were very good at developing their sub-systems and solving technical problems, but the needed interdisciplinary coordination proved very time consuming and slowed down the overall development. It might seem rather surprising that this came as a surprise since all space professionals who visited the team as guest lectures and advisors warned us about this. However, as always students are very persistent, enthusiastic, and optimistic so we equalised this with all the technical problems that also seemed overwhelming in the beginning.

As always *learning by doing* is a hard, but efficient, way of learning and we learned mostly a lot about how *not* to organise a large interdisciplinary project! However, ultimately we found ways to improve the organisation. The main organisation was coordinated from a system engineering group that have a representative from each sub-system group. This architecture was used from day one, but it took about a year before the group started working efficiently enough. An obstacle, different from the dominating focus on the technical part, is that it is not possible to give students academic credit for organisational work on DTU – apparently DTU only wants to set focus on theoretical management even though experience shows that management is much harder in practice. The lack of academic credit naturally had the effect that the students avoided the organisational work as much as possible, which made it even harder for the few students that actually involved themselves. Report(s) on how not to organise future DTUsats, and how to improve the organisation will probably become available within the next six months.

One of the goals on the list of *criteria of success* (page 3) was to give the students hands-on experience with management and organisation of large projects. This goal has most definitely been fulfilled, and the experiences will be brought on to future DTUsat students via reports and lectures. These lectures will be part of the introductionary course on satellite construction at DTU, which will also be used to pass on experiences from the developed sub-systems along with lectures from space professionals.

1.1.4 Launch

DTUsat was launched on June 30 2003 at 14:15:12GMT from Plesetsk, Russia to an altitude of 820km and a 97° inclination. Attempts to establish contact with the satellite was futile, which of course has been very frustrating for all the involved students because of the amount of time and personal efforts that was spent on DTUsat.

DTUsat was in the same P-POD as the other Danish student satellite AAU CubeSat from Aalborg University and the Canadian CanX-1 from

(a) (b)

Figure 1.6: *(a)* Launch of DTUsat from Plesetsk, Russia on June 30 2003 at 14:15:12GMT. *(b)* Animated picture of DTUsat in orbit; an animation of antenna deployment in orbit can be found on the enclosed CD-ROM (©2003 Danish Space Research Institute (DSRI)).

Toronto University, Canada. Only AAU CubeSat was able to establish radio contact – however, a very reduced bandwidth was experienced and communication was very unstable, which had the effect that only very simple telemetry like battery voltage was received.

Since communication with DTUsat failed and thus no debugging information was retrieved, and since both flight and flight spare performed flawlessly on the ground, we cannot conclude what went wrong. However, one thing that is for sure is that the available time for integration and testing was too short since only $1\frac{1}{2}$ months was available before the P-POD integration deadline. The difference in the level of success between DTUsat and AAU CubeSat can be explained by the fact that AAU CubeSat is more simple and that they had a better organisational structure, which then left them more time for testing.

Even though the satellite did not fulfill its scientific mission, the main goals of the project were still achieved. The first five points from the list of *criteria of success* (page 3) has been fulfilled as described above and in the previous sections.

1.1.5 The Future for DTUsats

A higher level of success would most likely have been obtained if the satellite had been a KISS (Keep It Simple, Stupid) CubeSat. However, this was not possible since all students insisted on designing and constructing very advanced sub-systems – and since it was a student satellite the students had to make the decision themselves. The positive side of the high level of ambitions is that very versatile high performance sub-systems is available as starting points for future missions – if one look at the many CubeSats that has been designed, but not yet launched, around the world one will find that

DTUsat is one of the most ambitious.

Future DTUsat missions will, oppositely to what many uninitiated students might think, require more than just plugging the existing sub-systems up and doing a lot of testing. All sub-systems have been documented, and the ideas from the reports together with new ideas can be used to make the systems better and even more flight compatible.

It is the intention to launch a DTUsat every second year as part of a new specialisation in space engineering that starts in the autumn of 2004. A DTUsat-II based on the experience and sub-systems obtained from DTUsat will most definitely have a much higher level of success in orbit.

1.2 The Sun Sensor Now and in the Future

The sun sensor that is the topic of this report has a performance that is comparable with commercial devices with a mass in the 200-500g range. The high mass means that these are not useable for CubeSats and thus justifies the need for the developed sensor. The sun sensor has been presented at the conferences listed below, and from these and the literature we can conclude that our device is the smallest sun sensor today. In section 2.2 an overview of current MEMS sun sensors is given. During the duration of this project the following articles have been presented at conferences:

16th Annual AIAA/USU Conference on Small Satellites
August 12-15, 2002. Utah State University, Logan, USA
Title: *Two-Axis MOEMS Sun Sensor for Pico Satellites* [13]
Authors: J.H. Hales and M. Pedersen

At this conference the authors participated in a student competition where a 4th place was obtained among 34 projects.

ESA's 4th Round Table on Micro/Nano Technologies for Space
May 20-22, 2003. ESA/ESTEC, Noordwijk, The Netherlands
Title: *Two-Axis MOEMS Sun Sensor and MEMS Electron Emitter Developed at MIC for DTUsat* [9]
Authors: R.W. Fléron, M. Pedersen, J.H. Hales, P.R. Bidstrup, and A. Torp

54th International Astronautical Congress
September 29 - October 3, 2003. Bremen, Germany
Title: *Linear Two-Axis MOEMS Sun Sensor and the Need for MEMS in Space* [35]
Authors: M. Pedersen, J.H. Hales, and R.W. Fléron

In this paper a discussion of why MEMS technology is a well suited technology for space applications is given. The reader is referred to appendix J to read about this.

ESA sponsored our participation, accommodation, and transport for this conference through their student outreach programme.

These articles can be found in appendix J. Furthermore the authors have participated in the following conferences:

World Space Congress 2002

October 10-19, 2002. Houston, Texas, USA

World Space Congress is the largest space conference and it is an event where everybody from the space community meet every 10 years when the IAF/IAC, COSPAR, AIAA, IAA, and UN conferences coincide. At this conference we were Danish delegates at Space Generation Summit – a summit under Space Generation Advisory Council (SGAC), which cooperates with UN to establish politics for peaceful utilisation of space.

ESA sponsored our participation, accommodation, and transport for this conference through their student outreach programme.

1st Danish Student Space Workshop

March 26-28, 2004. Copenhagen, Denmark

Speakers on MEMS in Space.

The presentations of the sun sensor have had the delightful consequence that the device is not doomed to a desk drawer destiny! At the conferences our ideas of bringing more MEMS into space have been well accepted. As it will become apparent in the subsequent chapters a lot of work is still needed before the sun sensor is fully space qualified. Nevertheless, following projects have already shown interest for the sensors:

SSETI Express

Microsatellite. Precursor for the SSETI mission. ESA funded missions. Current status: sensors about to be integrated at ESA/ESTEC, Noordwijk, The Netherlands.

COMPASS-1

CubeSat from the University of Applied Sciences Aachen, Germany.

Students at Aachen are currently performing vacuum testing on our sensor as a step in the space qualification process – contact: M.Sc. Student Jens Giesselmann.

AAU CubeSat II

CubeSat from Aalborg University, Denmark. No sensors delivered yet.

DTUsat-II

Well, actually we have not yet delivered sensors since the project will not be initiated before autumn 2004, but we feel quite confident that we will also fly on DTUsat-II. Actually some sun sensor testing have already been initiated by M.Sc. Student Lennart Vass Petersen at Ørsted•DTU.

Hopefully the contributions and flight data from these missions will help the sensor surviving and being used on many – especially nano and pico – missions in the future.

1.3 The Scope & Outline of this Report

This report is mainly written for engineering students who wants to continue the work on the sun sensor. Therefore the majority of the report is written so that persons with a wide knowledge within polytechnics can use it for continued development. The parts involving semiconductor technology will however go into a more detailed treatment that requires some specialisation.

The realisation of the design ideas in the clean room has been the most challenging and time consuming problem of the project. This means that the emphasis in this report is on the design, realisation, and validation whereas the testing part is not complete since only design validation and initial testing was started in this project. As described in the previous section it is our hope that the space qualification tests, which is a huge project in itself, will be continued by others.

The report is divided into the following chapters before the conclusion and appendices:

2 Device Principle
The principle of the sun sensor is described, and an overview of other groups' work with MEMS sun sensors is given.

3 Device Design
Describes the needed theory, the design of the physical dimensions of the device, the performance of the ideal sensor, design of the pn junction, and optical considerations.

4 Process Design & Validation
In this chapter the mask and process design is treated along with validation of the clean room processing. Application engineers may skip this chapter.

5 Electronics Design & Mechanical Integration
The electronic design and mechanical integration on DTUsat is described.

6 Performance Evaluation
An evaluation of the sensor principle is given along with a discussion of the obtainable resolution and a description of the test setup. An initial quantum measurement is described as well as the evaluation of the IV characteristics. Finally the calibration of the sensor and the correlation to magnetometer measurements is briefly described.

2

Device Principle

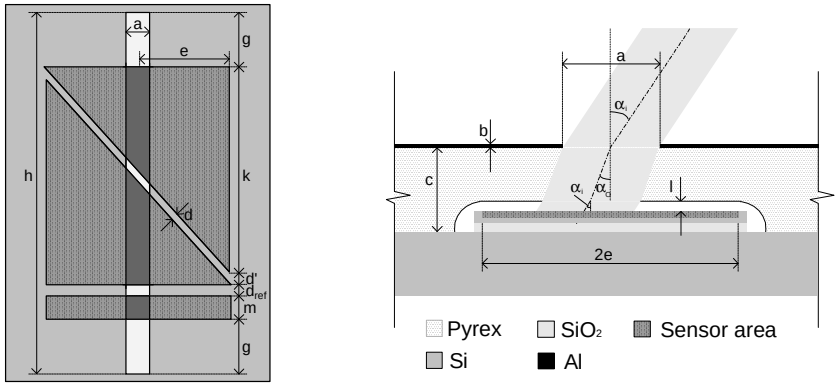
The purpose of a sun sensor is to assist in the determination of the attitude of a spacecraft. For orbiting satellites the case is simpler since complete attitude determination is achievable with the exception of the rotation around the sun vector – if we of course assume that the satellite is exposed to sun light. This is done by measuring the satellite-sun vector, and using that the earth-sun vector can be calculated from the time and that the earth-satellite vector can be found from the time and the orbit parameters of the satellite. From these the attitude of the satellite with respect to Earth can be determined – usually defined by a rotation matrix or a quaternion.

A description of the sensor principle chosen for the project at hand along with an overview of other MEMS sun sensors available today are given in this chapter.

2.1 Sensor Principle

The sensor principle for the developed sensor was chosen in our B.Sc. thesis project which was carried out in collaboration with M.Sc. Student K. Krogsgaard [14]. An analysis of e.g. various approaches can be found in [14]. The chosen sensor type is a two-axis analog slit sensor with triangular photodiodes. Figure 2.1 depicts the principle design of one axis.

Better resolution is achievable with a pin-hole mask on top of a CCD (Charge Coupled Device) or APS (Active Pixel Sensor) chip. This solution do however require more electronics and mounting a pin-hole mask on top of a commercial CCD/APS would increase the overall size of the sensor itself – by processing our own combined CCD/APS pin-hole chip the size could be lowered, but doing this is not possible in the available clean room. The simpler analog slit sensor was chosen due to mass, dimensional constraints, and the invariable requirement for having devices finished in time before the launch of DTUsat.



(a) (b)

Figure 2.1: Sketch of one axis of the analog triangular slit sensor. *(a)* Top view. *(b)* Cross sectional view.

As depicted in figure 2.1 the sensor is realised with a Silicon On Insulator (SOI) – Pyrex sandwich structure. The Pyrex (borosilicate glass) part acts as a lid where sun rays only enter through the slit, and the SOI wafer contains the needed photodiodes. The difference between the generated photocurrents in the triangular diodes is used to find the angle of the incoming sun rays, and the current from the rectangular reference cell is used to eliminate various unwanted parameters.

By placing two one-axis sensors perpendicular to each other – as seen in the chip layout in figure 2.2 – a two-axis sensor is realised. The sensor chips flying on DTUsat are $7 \times 8\text{mm}^2$ and weighs 116mg.

A SOI wafer is used since it enables complete electrical insulation by etching away the top mono-crystalline Si-layer. These grooves are created between all diodes and are continued all the way through the oxide layer to the bulk-Si to allow anodic bonding of the sandwich structure; the SOI structure also prevents e.g. Na contamination of the device layer.

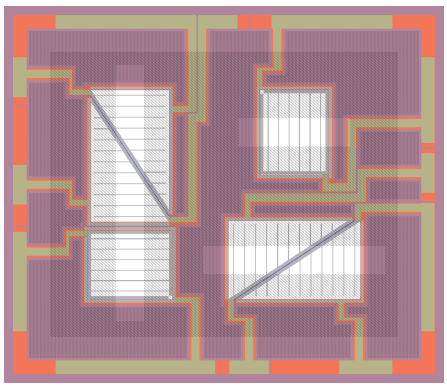


Figure 2.2: Chip layout of the two-axis triangular slit sensor.

The cosine factor of the ideal photo current is given by $\cos(\alpha_k)\cos(\alpha_e)$ where α_j are the sun rays' angles about the k and e axes (cf. figure 2.1). By selecting the length g large enough the illuminated area is made independent of the α_e angle.

DTUsat is a CubeSat and hence cubic [39], which means that complete coverage can be obtained by designing for ±FOV (Field Of View) larger than $\arctan(\sqrt{2a^2}/a) \approx 55^\circ$ and placing one two-axis sensor on each side. This was an initial requirement [14]; however later for structural reasons it was decided to omit sun sensors on the payload side. The final FOV is well above the initial requirement.

The reference areas enables on-chip temperature measurements.

The reference area can furthermore be used as a temperature sensor. An angle measurement allows calculation of the sun power exposed to the sensor since the sun power is relatively constant over time. By using this the temperature can be determined by knowing the sensors temperature dependence, which can be found to good precision both analytically and from measured characteristics. Knowing the temperature of the chip is useful for in-orbit validation of the sensor principle, and for housekeeping of the satellite environment.

2.1.1 Elimination of Undesired Parameters

The reference area can be used to cancel out several unwanted parameters. This is done by dividing the difference signal with the reference signal, and utilising that constant physical properties over the mono-Si layer can be assumed. The reference area has constant illuminated area (the considered angles in this section are all incoming angles – α_i in figure 2.1):

$$A_{ref} = (a-s)m\Big|_{s=b\tan(\alpha_k)} \approx am \tag{2.1}$$

since the shadow effect s of the slit can be neglected due to the low height b of the deposited metal (nm regime). If the difference between the generated triangular diode currents currents is used to find α_k then the result for the ideal case is ($\frac{P}{A}$ sun power per square metre, $A_t(\alpha_k)$ illuminated area of one triangle, $V(T)$ diode forward voltage, transmission term $(1-R(\alpha_k,\alpha_e))$, and η the efficiency):

$$\begin{aligned}
\frac{\Delta I}{I_{ref}} &= \frac{I_{t2}-I_{t1}}{I_{ref}} \\
&= \frac{\frac{P}{A}\cos(\alpha_k)\cos(\alpha_e)}{V(T)}\left(1-R(\alpha_k,\alpha_e)\right)\eta\left(A_{t2}(\alpha_k)-A_{t1}(\alpha_k)\right) \\
&\quad \frac{\frac{P}{A}A_{ref}\cos(\alpha_k)\cos(\alpha_e)}{V(T)}\left(1-R(\alpha_k,\alpha_e)\right)\eta \\
&= \frac{A_{t2}(\alpha_k)-A_{t1}(\alpha_k)}{A_{ref}}
\end{aligned} \tag{2.2}$$

From this it is seen that the sensor can be made independent of the cosines and the temperature in $V(T)$ (the most significant temperature dependence of solar cells). Cancelation of $V(T)$ also removes most dark current effects, and cancelation of η removes dependence of sensor degradation due to radiation. Elimination of $\frac{P}{A}$ cancels disturbances caused by sun power fluctuations, and the albedo intensity contribution.

The angular disturbance from albedo is minimised by having maximum sensitivity in the short wavelength regime. More info on this can be found in section 3.2.3-3.2.4. In section 3.2.1 it can be seen that the transmission term $(1 - R(\alpha_k, \alpha_e))$ does not have a characteristic effect in the individual diode response for the selected FOV.

The output is only *a function of the illuminated chip areas.*

When the method illustrated in (2.2) is used the output signal is only a function of the illuminated areas in the ideal case. This makes the sensor more sensitive than if only the cosine dependence was used, and it furthermore allows a close to linear output as discussed in chapter 3. The main advantage of the principle is naturally that no environment calibration of the output is needed in the ideal case.

2.2 MEMS Sun Sensors Available Today

Among the very first MEMS sun sensors.

When the design of the sun sensor was initiated late 2001 no references to other MEMS sun sensors were found. However, in 2001 an article by researchers from NASA JPL was presented [25]. This article has the title *MEMS Based Sun Sensor* and describes a sun sensor constructed with a commercial APS chip. Whether the sun sensor should be called *MEMS* can be discussed since their aperture mask is mechanically fixed to the APS. Later in 2002 [26] and 2003 [30] the device do however become a real MEMS device. An additional paper regarding the image processing on the APS data has been presented [31]. Finally in 2004 there was a note about the device in NASA Tech Brief which showed the final specifications [2]. NASA JPL suggests use of the device for miniature spacecrafts and planetary robotic vehicles. In the conclusion of this report our device is evaluated with respect to this device.

Another MEMS sun sensor was presented in 2002 by researchers from Uppsala University, Sweden [3]. This device is fundamentally different from ours and NASA's since the main goal here is to obtain an extremely high FOV $> 2\pi$ steradians with the aid of a dome construction. The sensor is planned to be part of the NanoSpace-1 satellite which will make extreme use of MEMS technology [5, 37].

The trend at the moment for professional missions seems to be APS based sun sensors in the +200g range – from e.g. TNO TPD [38]. Work on miniaturisation of APS sun sensors is being conducted at the University of Naples, Italy [6] – however, not to the same extreme as at NASA JPL.

If the reader wishes to compare our MEMS version of a traditional design a traditional triangular slit sensor (without reference areas) has been developed by Surrey Satellite Technology Ltd. [27, 44, 43].

3

Device Design

This chapter will go through the basic theory needed for understanding the functionality of the semiconductor device, the physical design of the device, and the performance of the ideal sun sensor.

3.1 Basic Theory

An introduction to the basic theory needed for understanding the developed device is given in the following. The interested reader may gain more insight to semiconductors through modern text-books such as [32, 18], and insight to photovoltaics in classical books as [34, 11, 29, 20].

The photosensitive areas described in chapter 2 is in principle pn junction solar cells. In this report we will however simply denote them photodiodes since we are naturally not that concerned with efficiency[1]. A pn junction consists of: a n-doped part where one extra valence electron exists for each substitutional donor atom, and a p-doped part where there is one valence electron less per substitutional acceptor atom (compared to the number of valence electrons in the undoped material). This can as in our case be realised with e.g. silicon (Si $\in$ group IV, four valence electrons) with impurity atoms from group V and III for donor and acceptor atoms respectively. This is illustrated in figure 3.1.

At low temperatures the donor electron is bound to the donor atom, P. The energy required to elevate the extra electron to the conduction band is naturally much lower than the energy needed to elevate one of the four electrons in the high-energy covalent bonds. When the electron is elevated to the conduction band it leaves behind a positively *ionised* donor impurity atom. Similarly at low temperatures there is a missing covalently bonded

[1] In some textbooks the term *photodiode* is exclusively used for pn-junctions operated in reverse bias modes. To avoid confusion it must be noted that in the sun sensor application the diodes are operated as solar cells.

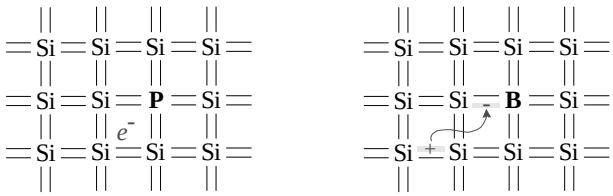


Figure 3.1: 2D representation of doped Si lattices. *(a)* n-type silicon crystal doped with phosphorus. *(b)* p-type silicon crystal doped with boron. The figure depicts the ionised situation where an electron has gained enough thermal energy to move to the acceptor atom (loosely bound valence electron).

electron in the lattice point where the acceptor atom resides. The energy of an electron in this position is naturally a little higher than the energy in a normal Si-Si covalent bond since the net charge of an occupied acceptor atom would be negative. When the 'empty' position becomes occupied by an electron the atom is denoted an *ionised* acceptor impurity atom and the positively charged point left behind is denoted a hole – in transport theory one regards these holes as particles since the description of these are simpler than the electrons' in p-type materials. The energies needed for donor and acceptor ionisation are in the same range and are low enough to allow thermal ionisation. The possibility of thermal ionisation is the reason why semiconductor devices are normally operated in the complete ionisation regime where all donor and acceptor atoms are ionised. The ionised donor/acceptor impurity atom concentrations are denoted N_A and N_D and are the same as the donor/acceptor impurity atom concentrations in complete ionisation. Complete ionisation is assumed in the following.

Figure 3.2 shows the situation when a p- and n-type material is brought in contact. Naturally they are not "brought in contact" in a physical sense today since they are created using planer processing – however, the descrip-

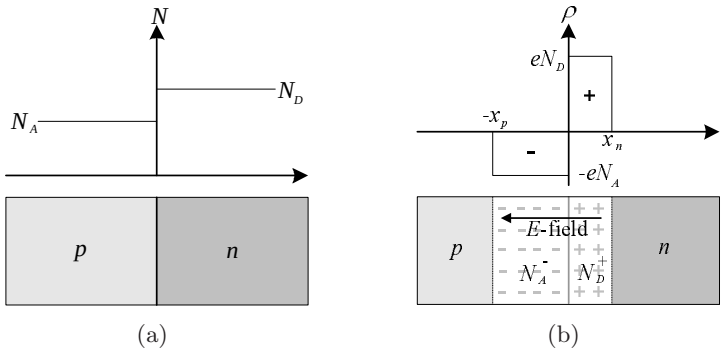
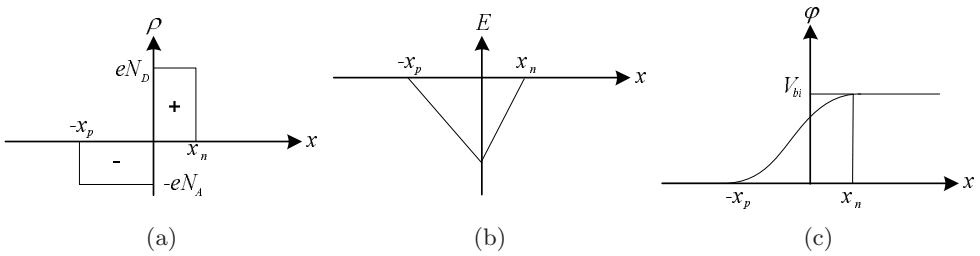


Figure 3.2: *(a)* A pn-junction before diffusion has started. *(b)* After diffusion a depletion/space charge region is created.



(a) (b) (c)

Figure 3.3: *(a)* Charge density, *(b)* electric field, and *(c)* electric potential in the space charge region of a uniformly doped pn-junction with the abrupt junction approximation.

tion is still valid. The p-side has a larger hole concentration than the n-side and the n-side has a larger concentration of conduction electrons. This causes a diffusion of holes to the n-side and of electrons to the p-side. This process builds up a permanent electric field from the surplus of positive and negative charge in the n- and p-side (cf. figure 3.2(b)), and the process stops when the forces on the particles from the electric field equals the diffusion forces. The region that is affected by this process is called the space charge or depletion region, and it is the properties in this region that determines most of the characteristics of the diode.

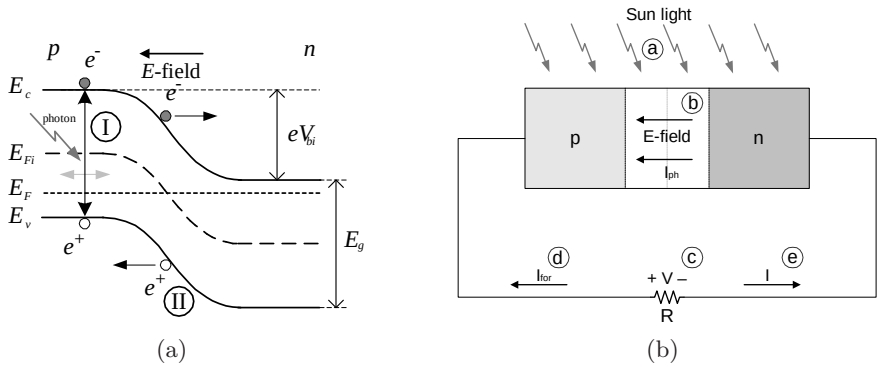
Assuming that we have the abrupt junction in figure 3.3(a) we can find the electric field in the space charge region by integrating Poison's equation,

$$\boldsymbol{\nabla}^2\phi = \frac{-\rho}{\epsilon} = -\boldsymbol{\nabla}\boldsymbol{E} \tag{3.1}$$

where ϕ is the electric potential, ρ the charge density, and ϵ the dielectric constant. Figure 3.3(b) shows the result of the integration. Integrating once more gives us the electric potential shown in figure 3.3(c). The potential energy of an electron is $-e\phi$ and using that along with the fact that the Fermi energy (the energy where all states below are filled with electrons and all states above are empty at $T = 0K$) must be constant through the device gives us the band diagram shown in figure 3.4(a).[2] Here E_c is the conduction band, E_v the valence band, E_{Fi} the Fermi energy of the intrinsic (undoped and no lattice defects) semiconductor, E_F the Fermi energy, and V_{bi} the built-in potential. eV_{bi} is the energy barrier that prevents electrons from the n-side in entering the p-side, and holes from the p-side in going to the n-side.

This band diagram can be used to understand the principle of the photodiode. What happens is that when a photon enters the device with energy $h\nu$ larger than the bandgap energy E_g it might interact with a valence electron and elevate it to the conduction band (**I** in figure 3.4(a)) – note that

[2]Note that $\boldsymbol{E}$ (bold) denotes an electric field vector and just E denotes an energy. An exception is however given in figure 3.3(b) where the E denotes the 1D electric field in the 1D case.



(a) (b)

Figure 3.4: *(a)* Band diagram of a pn-junction in equilibrium. *(b)* pn-junction photodiode.

this process may happen everywhere (p-side, space charge region, and n-side) and that the probability of interaction is high since the valence band contains many electrons and the conduction band many vacant places. This creates an electron-hole pair that moves around due to Brownian motion and diffusion[3] – one should note that the pair-particles are not bound together since there are more electrons and holes in the material to relieve them from the electrostatic attraction, but thinking of them as a pair is still useful. When the pair comes close to the space charge region the electric field inhere will separate the pair as indicated at **II** in figure 3.4(a). The holes are swept into the p-region and the electrons to the n-region. In these regions the new carriers are majority carriers, which means that they are now recombination-free since no recombination possibilities exist. The accumulation of majority carriers enables us to utilise the generated carriers by driving a reverse biased external current by connecting the p- and n-side through a load as indicated in figure 3.4(b). What actually happens here is that we move the extra electron from the n-side to the p-side where it recombines with the extra hole.

Having clarified these physical properties the principle of a pn junction photodiode can easily be described (cf. figure 3.4(b)):

- **a)** Sun light hits the pn device which causes generation of electron-hole pairs.
- **b)** The electric field in the space charge region separates electron-hole pairs and enables a reverse bias photo current I_{ph}.

[3]On the p-side: assuming no recombination gives $\frac{\partial n}{\partial x} = 0$ at the connection electrode, and at the junction border we have $n = 0$ since all electrons here are swept to the n-side. This means that electrons will diffuse towards the junction. Due to charge neutrality and the oppositely directed electric from the n-distribution field the p-distribution will have a similar profile, but naturally an overall movement in the opposite direction. A similar argument is naturally valid for the holes and electrons on the n-side.

- **c)** I_{ph} results in a voltage drop V across the load R. This forward bias potential decreases the E-field in the pn device, but the field never reaches zero or changes direction.
- **d)** The potential causes a forward bias current I_{for}. Since the pn junction photodiode is a diode the current I_{for} can be found with the ideal diode equation: $I_{for} = I_s[\exp(\frac{eV}{kT}) - 1]$, where e is the charge of an electron, k Boltzmann's constant and T the temperature.
- **e)** $I = I_{ph} - I_{for}$ is then the net pn junction current.

3.1.1 Creation of Electron-Hole Pairs

The process of creating an electron-hole pair is a bit more complicated than indicated in the above text. In the simplest case we have a direct bandgap where only an energy of at least E_g is required to make an electron-hole pair – an example of a direct bandgap material is GaAs in figure 3.5. Since we have conservation of crystal momentum ($p = \hbar k$) we have $k_f = k_i + k_{ph}$, where k_i is the initial wave vector, k_{ph} wave vector of the photon, and k_f the final/resulting wave vector. Using this direct transitions might at first seem impossible, but since $k_{ph} = p/\hbar = 2\pi/\lambda$ is negligible compared to typical electron wave vectors (e.g. at a Brillouin zone boundary: $k = 2\pi/a$ where a is the lattice constant) we can regard the transition as being essentially vertical.

Indirect bandgaps as in e.g. silicon is the other transition case. In addition to the required energy E_g we also need a phonon interaction with wave vector $\pm k_{phonon}$ to create an electron-hole pair – the $\pm$ refers to phonon

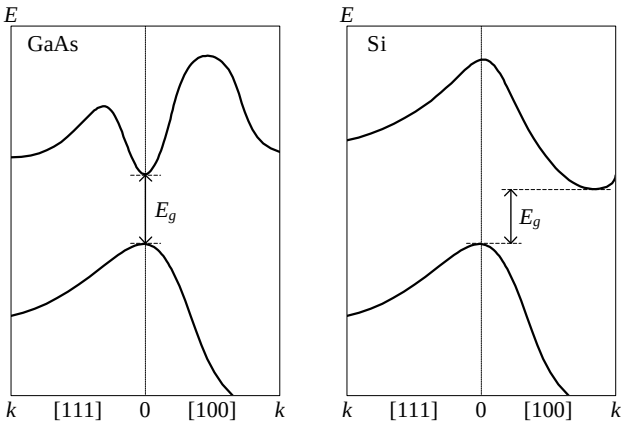


Figure 3.5: Sketch of the energy band structures of GaAs and Si. Only the lower conduction and upper valence band is sketched to illustrate direct (GaAs) and indirect bandgaps (Si). [111] and [100] are the only crystal directions included because the lowest conduction band minima occur here.

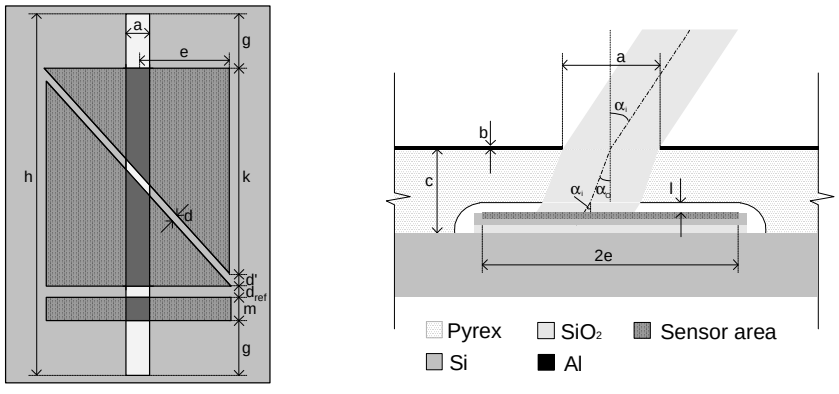
absorbtion/emission. In this case the photon actually needs the energy $h\nu = E_g \mp h\nu_{phonon}$ depending on needed absorbtion/emission. The phonons come from thermal lattice vibrations. At high photon energies vertical transitions between the valence and conduction band will dominate over phonon assisted transitions because of the simplicity of the pure photon interaction.

3.1.2 Limitations of Efficiency

The description in the preceding text assumes that we are operating a perfect photodiode. However, in practice there is naturally several limiting factors which we will not go into depth with since are not interested in high efficiency. For example recombination may occur before the electron-hole pair is separated in the space charge region, which means that the closer the pair is generated to this region the higher is the possibility for survival. One practical solution to this problem is to make multi-junction devices with junctions at different depths for different photon wave lengths. Prolonging the minority carrier life times and minimising the number of recombination traps within the bandgap are examples of design goals if high efficiency is wanted. Coating of the surface helps minimising the number of surface traps and increasing of the optical absorbtion. For the sun sensor an optical coating is used to make the device more sensitive at short wave lengths – see section 2.1.1 for the principle and section 3.2.4 for how the optical filter is implemented.

3.2 Sensor Design

This section describes the overall physical design of the two-axis triangular slit sensor. The more detailed process design is described in chapter 4 and



(a) (b)

Figure 3.6: Sketch of one axis of the analog triangular slit sensor. *(a)* Top view. *(b)* Cross sectional view.

more details on the mask design is given in section 4.1. The principle design of one axis of the sensor (cf. chapter 2) is repeated in figure 3.6. As explained in chapter 2 two of these one-axis sensors are to be placed perpendicular to each other on the sensor chip to realise the two-axis sensor. Figure 3.7 shows the mask layout of the final chip.

3.2.1 Dimensioning & Ideal Current Characteristics

By considering $\Delta I/I_{ref}$ from (2.2) we see that the illuminated area $A(\alpha_k)$ naturally is the parameter in which the physical dimensions of the sensor play a role. In general we see that the current of one of the chip's six photodiodes are given by (reusing the introduced symbols in section 2.1.1):

$$I = \frac{\frac{P}{A}\cos(\alpha_k)\cos(\alpha_e)}{V(T)}\left(1 - R(\alpha_k, \alpha_e)\right)\eta A(\alpha_k) \tag{3.2}$$

The sensor has three different photodiodes as seen in figure 3.6. Expressions for the illuminated areas are found by considering the geometry; a more thorough derivation can be found in [14] where the chosen sensor principle was investigated. Expressions of the areas as functions of the dimensional parameters are – for increasing illuminated area $A_{t1}(\alpha_k)$ and decreasing $A_{t2}(\alpha_k)$:

$$A_{t1}(\alpha_k) = (a-s)(2e + 2(c-l)\tan\alpha_{ko} + 2l\tan\alpha_{ki} + s)\frac{k}{4e} \tag{3.3}$$

$$A_{t2}(\alpha_k) = (a-s)(2e - 2(c-l)\tan\alpha_{ko} - 2l\tan\alpha_{ki} - s)\frac{k}{4e} \tag{3.4}$$

$$A_{ref}(\alpha_k) = A_{ref} = (a-s)m \tag{3.5}$$

where $s = b\tan(\alpha_{ki})$ is the shadow effect from the height of the deposited slit metal – note that since b is in the nm regime the effect is not pronounced.

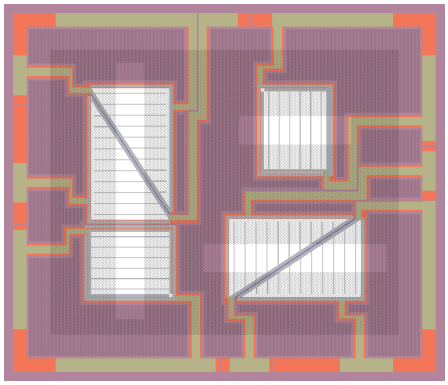


Figure 3.7: Chip layout of the two-axis triangular slit sensor.

Equation (2.2) in the ideal case (increasing $A_{t1}(\alpha_k)$ and decreasing $A_{t2}(\alpha_k)$) can be found by using (3.3)-(3.5):

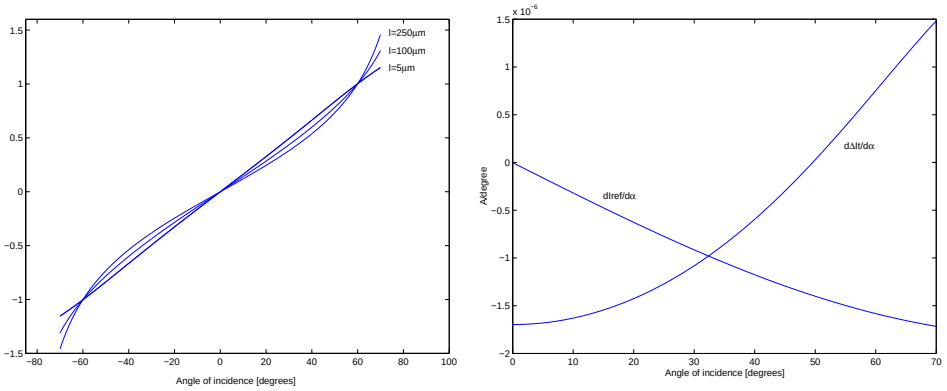
$$\frac{\Delta I}{I_{ref}} = \frac{(-2(c-l)\tan\alpha_{ko} - 2l\tan\alpha_{ki} - s)k}{2em} \qquad (3.6)$$
$$\alpha_{ko} = \arcsin\left(\frac{n_1}{n_2}\sin(\alpha_{ki})\right)$$

where $s = b\tan\alpha_i$ is the shadow effect from the slit. α_{ko} (cf. figure 3.6(b)) is found by simple optical considerations and n_1/n_2 are the refractional indices for vacuum/Pyrex.

The size of a, e, k, and l are important for the final characteristics of the device. Values used for the dimensioning of the device are: diode forward voltage $V(T) = 0.7\text{V}$, efficiency $\eta = 0.1$, and average sun intensity $\frac{P}{A} = 1371\frac{\text{W}}{\text{m}^2}$. η has been selected quite low since experience at MIC shows that $\eta = 0.16$ can be obtained quite easily. The sensor is dimensioned from a desired current of $100\mu\text{A}$ at $\alpha_k = 0°$, and by using the low η this signal should be ensured. Higher output signals give less noise problems, but causes an increasing device size. The parameter k is determined from the current requirement:

$$I_{t,0°} = \frac{\frac{P}{A}\frac{1}{2}ak}{V(T)}\eta(1 - R(0°, \alpha_e)) \quad \Leftrightarrow \quad k = \frac{2I_{t,0°}V(T)}{a\frac{P}{A}\eta(1 - R(0°, \alpha_e))} \qquad (3.7)$$

Large value of k ($\Rightarrow$ narrow slit length a) is desired for large changes in $A_t(\alpha_k)$, but contrarily wide a is needed for a small reference cell height m. m is also selected from the desired current at $\alpha_k = 0°$. e is given from the selected FOV which was selected to 70° which enables complete coverage on a CubeSat as explained in section 2.1. In section 3.2.1 below it is shown



(a) (b)

Figure 3.8: *(a)* $\frac{\Delta I_t}{I_{ref}}$ graphs showing that the Pyrex-sensor distance l influences the linearity. *(b)* Derivatives $\frac{\text{d}\Delta I_t}{\text{d}\alpha}$ and $\frac{\text{d}I_{ref}}{\text{d}\alpha}$.

that the reflectance $R(\alpha_k, \alpha_e)$ does not have a characteristic effect for this FOV.

Common for all measures is that they should cause relatively large $\frac{\mathrm{d}I}{\mathrm{d}\alpha_k}$ for most α_k to ensure high sensitivity. The larger the Pyrex-sensor distance l is the larger is the sensitivity for both the triangles and the reference area. However, larger l has the disadvantage that it increases the total chip size since a larger e then is required.

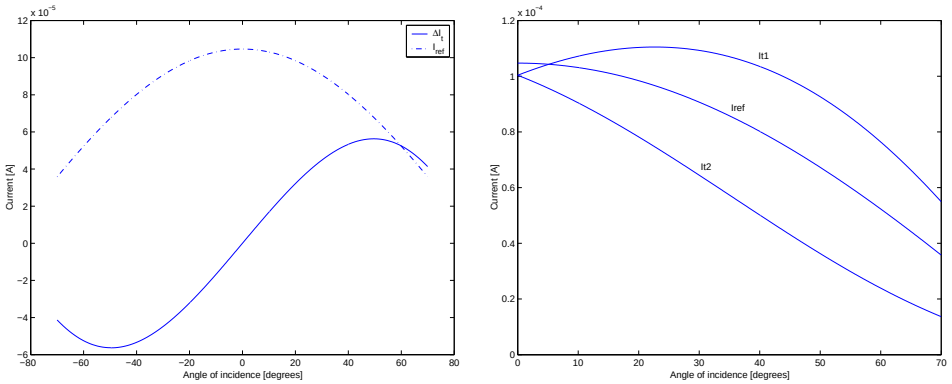
Non-linearity is introduced with $\tan(\alpha_{ki})$ since $\alpha_{ki} \geq \alpha_{ko}$ in equation (3.6); see figure 3.8(a). Therefore l should be selected as low as possible; however, since the Pyrex and SOI wafer are anodically bonded l should still be large enough to avoid bonding to the active sensor areas – and hence destruction of the pn junction.

This means that the size of l is a trade off between sensitivity on one side and total chip size and linearity on the other. Figure 3.8(a) indicates that the output is very linear for $l = 5\mu$m, and figure 3.8(b) indicates that a reasonable sensitivity is obtained for this l. The signals ΔI_t and I_{ref} are to be amplified with OPAMPs, and high quality OPAMPs have leakage currents in the order of 1nA, which means that we need at least 10nA/° to ensure high resolution by using these OPAMPs in simple circuits – this means that it should be possible to obtain a resolution better than 1° over the entire FOV. This is fulfilled everywhere except in a little interval around 0° for I_{ref} and around $\pm \sim 50°$ for ΔI_t. From figure 3.8(b) it is seen that the I_{ref} has a lower sensitivity than ΔI_t which is naturally due to the fact the reference area only has a cosine dependence whereas the triangles have a higher dependence because of the varying illuminated area. Regarding to chip size $l = 5\mu$m results in a total chip size of approximately $7\times8\text{mm}^2$ which was a size that fitted well into DTUsat for which the sensor was originally designed. More info on the obtainable resolution and the OPAMP circuit are found in chapter 5 and 6.

By evaluating the above trade offs and scaling the resulting measures

Description		**Value**	
Slit width	a	550	μm
Slit extra length	g	150	μm
Triangle height	k	2405	μm
Triangle width	$2e$	1505	μm
Reference area height	m	1190	μm
Sensor-Pyrex distance	l	5	μm
Pyrex thickness	c	500	μm
SOI device-Si thickness		5	μm
SOI oxide thickness		1	μm
Pyrex etching depth		11	μm

Table 3.1: Dimensions of the sun sensor.



(a) (b)

Figure 3.9: Ideal current plots for the chosen geometry. *(a)* ΔI_t and I_{ref}. *(b)* I_{t1} for increasing A_{t1}, I_{t2} for decreasing A_{t2}, and I_{ref}.

when drawing masks the design phase ended with the values shown in table 3.1. The chosen values result in the rather conservative design of a $7 \times 8\text{mm}^2$ chip, and the reason for choosing this design was the available time for development and production and the need for first time success.

Figure 3.9 shows plots of the ideal current characteristics for the chosen geometry, and figure 3.8(a) shows the linear $\Delta I_t / I_{ref}$ output from (3.6). The zero points in the sensitivity graph (figure 3.8(b)) is naturally the turning points in the current plots (figure 3.9(b)).

Reflection and Field of View

Even though the reflection is canceled out in (2.2) and (3.6) it should be noted that this is important for the actual amplitudes of the generated photo currents. The total reflection in the vacuum-Pyrex and the Pyrex-cavity transition of both the transverse electric and magnetic (TE/TM) polarised light waves can easily be deducted from the Fresnel equations:

$$R_{TE}(\alpha) = \left(\frac{\cos\alpha - \sqrt{n^2 - \sin^2\alpha}}{\cos\alpha + \sqrt{n^2 - \sin^2\alpha}} \right)^2 \tag{3.8}$$

$$R_{TM}(\alpha) = \left(\frac{n^2\cos\alpha - \sqrt{n^2 - \sin^2\alpha}}{n^2\cos\alpha + \sqrt{n^2 - \sin^2\alpha}} \right)^2 \tag{3.9}$$

where $n = \frac{n_1}{n_2}$. In TE/TM the $\boldsymbol{E}/\boldsymbol{B}$ vector is perpendicular to the plane of incidence, and the $\boldsymbol{B}/\boldsymbol{E}$ vector is in the plane of incidence. Light comes in equal portions of TE and TM modes, which means that the total reflectance

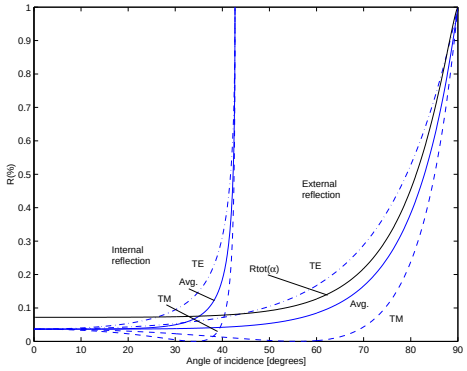


Figure 3.10: Reflectance in the vacuum-Pyrex transition (external), in the Pyrex-cavity transition (internal), and the total reflection.

in the sensor is[4]:

$$R(\alpha)_{lm} = \frac{R_{TE}(\alpha)_{lm} + R_{TM}(\alpha)_{lm}}{2}$$
$$R_{tot}(\alpha) = 1 - (1 - R(\alpha_i)_{12})\,(1 - R(\alpha_o)_{21}) \tag{3.10}$$

where subscript 12 and 21 means vacuum-Pyrex and Pyrex-cavity transition respectively. Figure 3.10 shows the above described reflections.

From figure 3.10 it is seen that the desired FOV $= 70°$ is obtainable since the total reflection still is relatively low at this point – $< 25\%$. At the same time the figure shows that aiming for a much higher FOV is pointless since the reflection increases rapidly after $70°$.

Deflection of the Cavity during Anodic Bonding

The maximum deflection of an $\tilde{a} \times \tilde{b}$ plate with its four sides fixed are given in [45]:

$$y_{max} = \frac{\tilde{\alpha} F \tilde{b}^4}{E t^3} \tag{3.11}$$

where F is a uniform force on top of the entire Pyrex cavity, $\tilde{b}$ the length of the short sides in the rectangle, $E = 64$GPa Young's Modulus for Pyrex, and $t = c - l$. $\tilde{\alpha}$ can be determined from tables in [45] to $\tilde{\alpha} = 0.0188$ since $\frac{\tilde{a}}{\tilde{b}} \approx 1.22$ for the sensor. An expression for the force F is deduced in [40]:

$$F = -\frac{\epsilon_g A V^2}{\left(\frac{1}{2}x_d + \frac{\epsilon_g}{\epsilon_0}x_r\right)^2} \tag{3.12}$$

[4]It is assumed that the reflected light in the Pyrex-cavity transition will not be reflected back in the vacuum-Pyrex transition.

where A is the area of the Pyrex cavity, V bonding voltage, $\epsilon_g = 4.6\epsilon_0$ permittivity for Pyrex, $x_d = 1\mu$m thickness of the depletion layer introduced with the bonding [40], and x_r which is the Pyrex-Si gap. Calculations give deflections in the order of $y_{max} = 4$pm. This shows that the Pyrex cavity will not be deflected to the sensor area and destroy it. That the vents (cf. section 3.2.2) in figure 3.7 has not been taken into account cannot change y_{max} with a factor 10^6, since the vents only constitutes a small part of the total bonding area.

3.2.2 Additional Structures on the Chip

In addition to the design of the cavity, slit, and sensor areas there are more structures in the final chip layout shown in figure 3.7 – in appendix B the different masks are shown individually. A special treatment of these structures will not be given since they are not specific for our application. Section 4.1 goes into some details about other parts of the mask design and section 4.2.3 gives an overview of how the chips are diced from the wafer – thinking this into the design is naturally quite important since tolerances allowing dicing etc. is required.

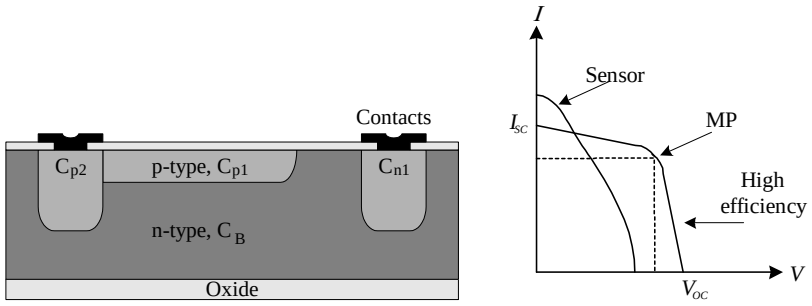
The most strikingly of the additional structures are naturally conduction paths and wire bonding pads. The only note that should be added here is that the bonding pads are made large enough to hold at least three wire bonds. The reason for this is that redundancy is wanted. For the chosen measuring principle it is not necessary to wire out connections to both ends of each diode since some of them could be connected on the chip. However, it was chosen to wire out all connections because it leaves the design more versatile for other principles.

For connecting the photodiodes two different approaches are included in the mask design. One where there is thin contact fingers over the active area to lower the resistance in the diodes. However, this has the disadvantage that it blocks out some light, which is why a version without fingers also was included.

Of the additional structures there is actually only one that is important to point out. Namely the cavities over all conduction paths, which are acting as vents when the sensor is exposed to vacuum in the space environment. Without these the sensor could explode, and it furthermore has optical advantages. The grooves in the SOI wafer for anodic bonding between the bulk-Si and the Pyrex wafer gives some auto alignment since the Pyrex parts without cavities automatically "falls" into these grooves.

3.2.3 Specifying the pn Junctions

Figure 3.11.a shows a schematic of the pn junction layout to consider when selecting the different concentration levels. Optimisation of the device aims



(a) (b)

Figure 3.11: Considerations regarding concentration levels. Picture *(a)* shows a schematic of the pn junctions in the device layer, where C_B is the background concentration of the device layer, C_{p1} is the concentration of the p-type area constituting one side of the resulting photodiode, C_{p2} and C_{n1} is the concentration of the layer below the metal contacts to the p- and n-type area respectively. Picture *(b)* shows the IV characteristic of an high efficiency solar cell under illumination and the sensor in question. The maximum power point (MP) is also shown.

at fulfilling the following points:

- High sensitivity in the UV-region
- Long carrier lifetime
- High photon sensitivity
- Reduce Schottkey barrier

As discussed in section 3.2.4 making the sensor more sensitive in the UV region will effectively decrease the angle inaccuracy due to albedo contributions. Creating a junction close to the surface will promote this UV sensitivity and can be realised by implanting a low dose at a low energy. Long carrier lifetime is desirable in order to ensure that a maximum of the electron generated by photons are collected. This is likewise achieved by having low concentrations of the device areas, yet at the cost of a higher series resistance as the resistivity increases for a decrease in impurity concentration. Low concentration levels will also ensure higher photon sensitivity since the resulting depletion width will encompasses the entire device layer according to equation (3.13). Thus almost all electron-hole pairs are created in the space charge region and subsequently swept to the terminals by the electrical field.

$$x_d = \sqrt{\frac{2\epsilon kT}{q^2}\left(\frac{1}{N_D}+\frac{1}{N_A}\right)\ln\left(\frac{N_D N_A}{n_i^2}\right)} \tag{3.13}$$

These considerations resulted in a C_B of 10^{14}cm^{-3} and a C_{p1} of $5 \cdot 10^{16}\text{cm}^{-3}$, which in part also is based on the available SOI wafers and the obtainable dose from the ion implanting facility where low concentration and energy is difficult to obtain due to mechanical constraints of the equipment. The values are two orders of magnitude lower than traditional high efficiency solar cells [32, 18] and results in the differences in the IV characteristic as sketched in figure 3.11.b. The purpose of a high efficiency solar cell is to deliver a maximum of power at a given voltage, hence the IV curve approaches the form of a square and has a lower I_{sc} due to lower depletion width which results in a weaker response for long wave lengths. Yet V_{oc} is larger as the electrical field in the depletion region is larger for the given concentration. The shape of the sensor IV characteristic shows that more energy is dissipated in the device due to the resulting higher resistivity, but has a favorable I_{sc} which is important for the photon sensitivity as discussed.

Schottky Barrier

A Schottky barrier is created when a metal is brought in contact with a semiconductor material as a result of the change in the energy band diagram in once thermal equilibrium. The barrier hight for a n-type $q\phi_{Bn}$ and a p-type $q\phi_{Bp}$ are:

$$q\phi_{Bn,p} = q(\Phi_m + \Phi_{n,p} - \Phi_s) \qquad \Phi_{n,p} = \frac{kT}{q}\left(\frac{N_{c,v}}{N_{D,A}}\right) \tag{3.14}$$

where Φ_m is the metal work function, Φ_s the work function of the semiconductor, $\Phi_{n,p}$ the potential difference between the Fermi level and the conduction/valance band, which has the effective density of states function given by $N_{c,v}$. Thus by increasing the impurity concentration under the metal contact (C_{p2}, C_{n1}) the barrier is lowered and a more ohmic contact is established and creating a more sensitive sensor. The realisation of this increase in concentration without considerably changing C_{p1} is described in section 4.2.

Process Sequence Simulation

The simulation software ATHENA-SSUPREM by Silvaco was employed to simulate how the above selected concentration levels diffuse during the thermal oxidation and to further visualise the resulting structure in terms of the oxide growth. Figure 3.12 shows the effect of the tree implantation steps also summarised in table 3.2.

Combining the information obtained for the resulting junction depth with Lambert's law of photon absorption written in equation (3.15) gives the percentage of photon absorbtion shown in figure 3.14, as the intensity

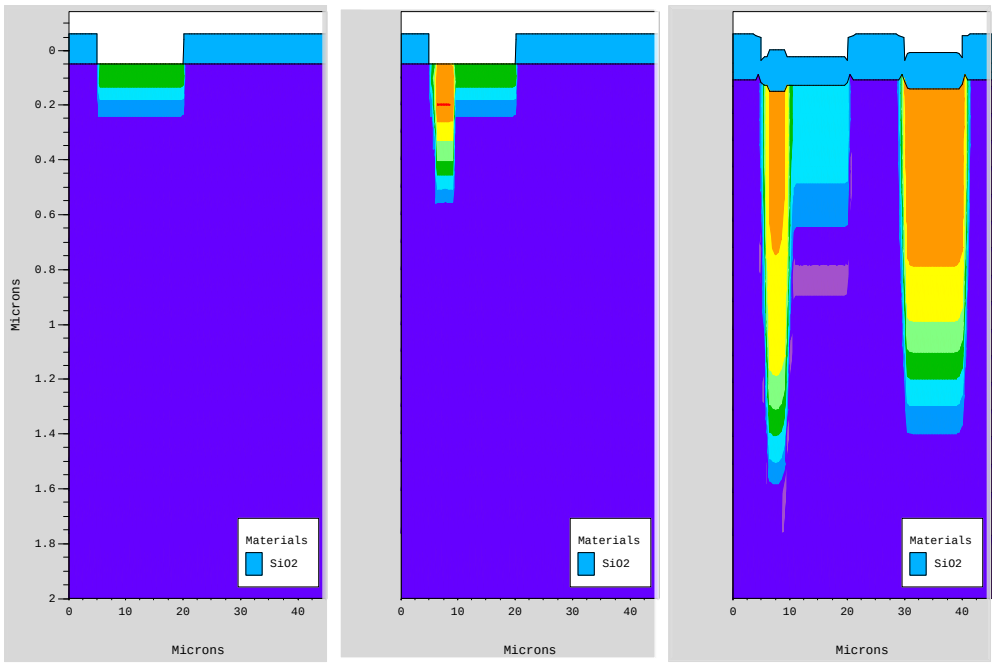


Figure 3.12: Structure plot of the three implantation steps where the concentration levels are contour plotted. From left to right the pictures show: low dose p-type followed by high dose p-type and finally high dose n-type

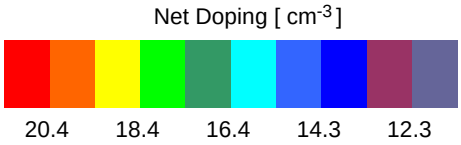


Figure 3.13: Concentration level legend for figure 3.12.

of the photon flux $I_\nu(x)$ at the position x:

$$I_\nu(x) = I_{\nu 0} e^{-\alpha x} \tag{3.15}$$

where the photon flux is denoted $I_\nu(x)$, $I_{\nu 0}$ the intensity of incident flux, and α the absorbtion coefficient of the specific material depending on wavelength. It is seen that the selected concentration levels promotes the goal of having a sensor less sensitive to the long wavelengths. An obvious improvement would be to grow the necessary oxide (employed of optical considerations described in 3.2.4 and as a pasivation layer) before implanting the impurities followed by an annealing step that is not governed by a desired oxide thickness, thus obtaining better control over the placement of the junction.

Impurity	Junction depth
Low dose p-type	0.17μm
High dose p-type	0.52μm
110nm of dry oxide grown at 1000°C for 200min	
Low dose p-type	0.66μm
High dose p-type	1.54μm

Table 3.2: Supreme results.

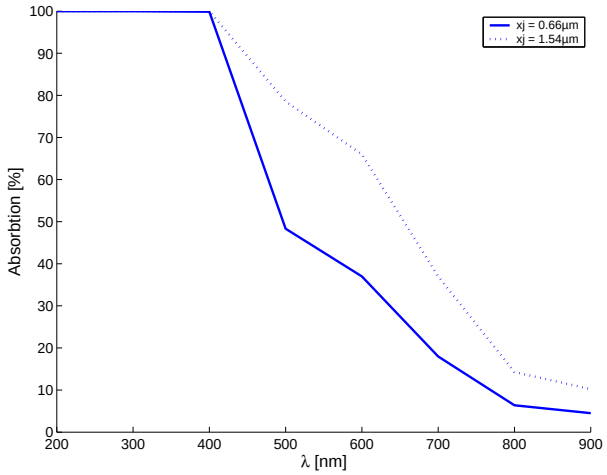


Figure 3.14: Percentage of photon absorbtion as a function of the wavelength for different junction depths.

3.2.4 Optical Considerations

The Earth albedo is defined as the percentage of the incident energy reflected back into space. This fraction is dependant of the time of year since e.g ice is more reflective than vegetation. An annual average is given to 29%, where the spectral characteristics are the same [42]. However the emitted radiation from Earth is dominant in the visual and infrared region. Making the sensor more sensitive in the UV region will therefore decrease the albedo associated angle inaccuracy.

To obtain this an optic filter is designed to either decrease the reflection in the UV region or increase reflection for all other relevant wave lengths.

This can be treated by looking at figure 3.15, where the reflection coefficient is given by the following relation for the electrical field[8]:

$$R = \left| \frac{E_{R0}}{E_{i0}} \right|^2 \tag{3.16}$$

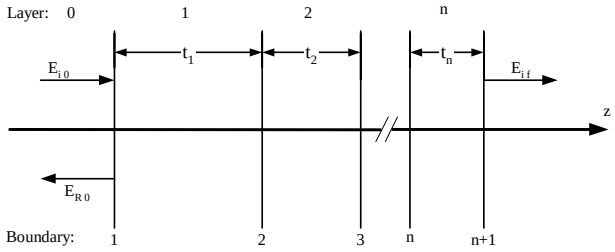


Figure 3.15: Multilayered optical structure.

Where the electrical field is expressed as:

$$\begin{bmatrix} E_{i0} \\ E_{R0} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & \frac{1}{n_0} \\ 1 & \frac{1}{-n_0} \end{bmatrix} \boldsymbol{M_1 M_2 ... M_n} \begin{bmatrix} 1 \\ n_f \end{bmatrix} \boldsymbol{E_{if}} \tag{3.17}$$

where (3.18)

$$\boldsymbol{M_P} = \begin{bmatrix} \cos(\psi_p) & -\frac{i}{n_p}\sin(\psi_p) \\ -in_p \sin(\psi_p) & \cos(\psi_p) \end{bmatrix} \tag{3.19}$$

and (3.20)

$$\psi_p = \frac{2\pi}{\lambda} n_p t_p \tag{3.21}$$

The constants n_p and t_p denotes the refractive index and the thickness of the relevant layer respectively. A structure consisting of a maximum of four different layers were considered due to process complexity – the top and bottom layer being vacuum and Si. Again to keep it simple the only considered additional layers were thermal SiO_2 and Si_3N_4, where the refractive index is well known and process compatibility is ensured. Selecting $n_1 t_1 = \lambda_0/4$ and $n_2 t_2 = \lambda_0/2$ minimises equation 3.17 with respect to λ_0 for the four layer structure discussed[5] [8]. Using these values results in the following expression where it should be noted that the electrical field does not depend on the properties of layer 3 (index 2) for λ_0.

$$\begin{bmatrix} E_{i0} \\ E_{R0} \end{bmatrix}_\lambda = \frac{1}{2} \begin{bmatrix} 1 & \frac{1}{n_0} \\ 1 & \frac{1}{-n_0} \end{bmatrix} \begin{bmatrix} 0 & -\frac{i}{n_1} \\ -in_1 & 0 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 \\ n_3 \end{bmatrix} \boldsymbol{E_{if}} \tag{3.22}$$

$$\begin{bmatrix} E_{i0} \\ E_{R0} \end{bmatrix}_\lambda = -i\frac{1}{2} \begin{bmatrix} \frac{n_3}{n_1} + \frac{n_1}{n_0} \\ \frac{n_3}{n_1} - \frac{n_1}{n_0} \end{bmatrix} \boldsymbol{E_{if}} \tag{3.23}$$

$$R = \left(\frac{n_3 n_0 - n_1^2}{n_3 n_0 + n_1^2} \right)^2 \tag{3.24}$$

Results of these design considerations are shown in figure 3.16 where λ_0 is selected within the UV range to 350nm.

[5] It is considered outside the scope of this report to show the minimisation.

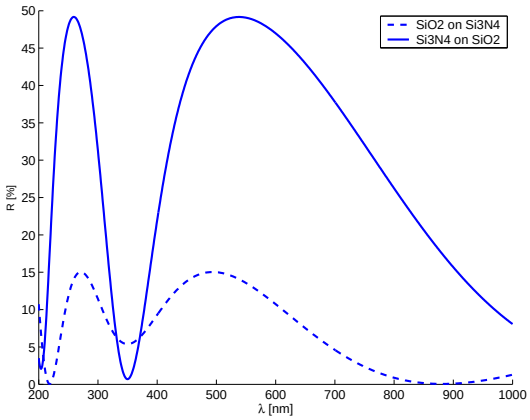


Figure 3.16: Sequence of nitride and oxide.

Having nitride on oxide gives a narrow window with high reflection outside λ_0 whereas the opposite situation results in a lower average but higher reflection for λ_0. Selecting one option over the other requires considerations of two main issues; stress and internal reflections.

Having layers of different material covering the whole wafer could introduce unwanted stress problems. It is therefore necessary to evaluate the total residual film stress σ for the two optical options. In the following calculation the parameters for thermal grown SiO_2 and stoichiometric Si_3N_4 are used.

$$\sigma_{totalstress,} = \frac{t_{oxide}\sigma_{oxide} + t_{nitride}\sigma_{nitride}}{t_{oxide} + t_{nitride}}$$

Option 1, oxide on nitride

$$\sigma_{option1} = \frac{\frac{\lambda_0}{4n_{oxide}}\sigma_{oxide} + \frac{\lambda_0}{2n_{nitride}}\sigma_{nitride}}{\frac{\lambda_0}{4n_{oxide}} + \frac{\lambda_0}{2n_{nitride}}}$$

$$\sigma_{option1} = 529\text{MPa}$$

Option 2, nitride on oxide

$$\sigma_{option2} = \frac{\frac{\lambda_0}{2n_{oxide}}\sigma_{oxide} + \frac{\lambda_0}{4n_{nitride}}\sigma_{nitride}}{\frac{\lambda_0}{2n_{oxide}} + \frac{\lambda_0}{4n_{nitride}}}$$

$$\sigma_{option2} = 73\text{MPa}$$

Having nitride as top layer is hereby shown to give the lowest residual stress, whereas having oxide on top could introduce stress problems. The residual stress is highly dependant on the fabrication method, implying the if one had to use Option 1, it would be possible to design a layer with lower stress. As an example the residual stress of stoichiometric Si_3N_4 is 1100MPa whereas for silicon rich Si_3N_4 varies from -50 to 800MPa [36]. However it

should be kept in mind that obviously the optical properties will also change if the material composition is altered.

Stress can greatly degrade or even destroy devices while internal reflection could result in inaccurate measurements. If incident light is reflected the only negative effect would be if it is re-reflected either by the Pyrex or by the Cr/Au. In that case the re-reflected ray could be absorbed by a sensor area and contribute to an angle offset. This effect could be mitigated by the fabrication of yet another antireflective layer on both the Pyrex and the Chromium layer. Physically applying such a layer is difficult due to the contaminating effects of free sodium ions in Pyrex. Thereby reducing the processing possibilities.

The possibility of using both nitride and oxide was first thoroughly investigated after the actual processing. Only oxide was considered as an antireflective layer. As a result of an error in the initial calculations the thickness of the oxide layer was chosen to 100nm. Resulting in the reflection shown in figure 3.17 where the optimal thickness of 60nm for a wavelength of 350nm also is shown. The optimal thickness has not been tried, but it is anticipated that the alignment marks will be harder to distinguish. This is a crucial point since the alignment marks at this point defines the contact holes, see appendix 4.

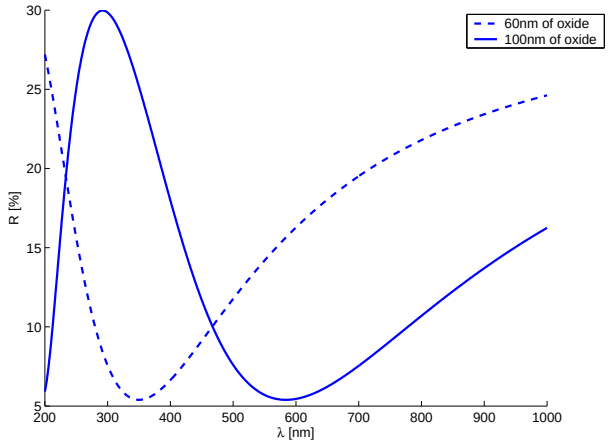
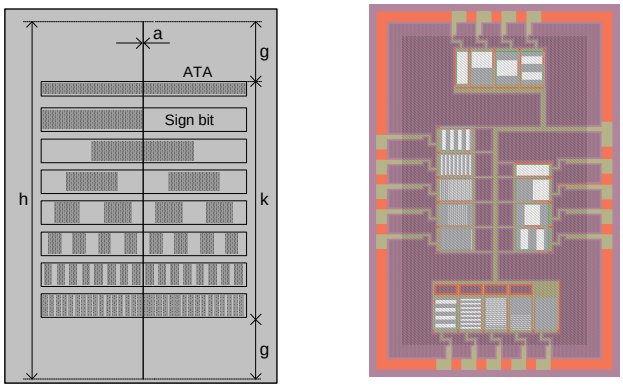


Figure 3.17: Optimal thickness of oxide compared to the actual.

3.2.5 A Digital Approach

Another type of slit sensor has been incorporated in the process and mask design. This sensor is a 8bit digital sensor utilising gray codes with a maximum accuracy of half a degree (for 70° FOV). The sensor principle relies on 1-2μm structure definitions requiring even more thorough processing which would result in prolonged fabrication time. Consequently a decision was



(a) (b)

Figure 3.18: *(a)* Sketch of digital sun sensor. Notice that the sensor implements Gray codes. The slit width a is smaller than the width of the LSB. *(b)* Masks for the 8bit digital sensor.

made to only focus on the analog sensor, even though the principle would be interesting to investigate further. The digital sensor will not be treated further in this report, however pictures are shown in some cases to underline certain process topics.

Figure 3.18(a) shows a principle sketch of the digital sensor, and figure 3.18(b) shows the mask layout. The sensor is made independent of albedo from the Earth and other dependencies by comparing currents from each bit with the ATA (Automatic Threshold Adjust) current. A bit is set if the generated current is the double of the ATA current since the ATA height is half the height of the bits. The sensor do however have the major drawback that its dimensions increases by $O(2^{n-1})$ with the desired bit resolution n. See [14, 41] for a detailed description of the sensor principle.

4

Process Design & Validation

As mentioned in the previous chapter, the fabricated device is a structure consisting of a Pyrex lid covering a SOI device area. Many different approaches have been tried in order to reach this goal. This chapter will give a brief overview of the actual fabrication process with references to the process sequence in appendix A, but will mainly focus on the considerations related to the critical steps of the process. Due to the nature of satellite construction, where time is a crucial factor, some of these considerations were made after the actual fabrication, but are included to suggest means of optimisation and to better explain or predict test results. Well proven process techniques have been used whenever possible in order to increase the possibility of fabricating a successful functioning device.

4.1 Mask Design

This section will describe the general mask layout based on the knowledge of the preceding sections where the chip itself was defined. The focus here will be on the considerations regarding the overall wafer layout and a description of incorporated test structures.

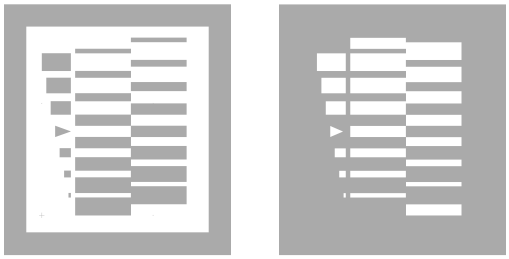
The mask layout is designed using L-Edit by Tanner EDA, which is a dedicated program for designing masks for micro technology. The actual drawing process will not be discussed except for the mask overview given in table 4.1. It shows the seven masks constituting the mask design, where also the alignment between the different masks are given. For additional insight to the mask layout should appendix B be consulted, which shows all the different structures in the mask design along with an overview of each mask.

Besides yielding the constraints and requirements from section 3 the masks have to consist of different test structures for verification of critical process steps.

Mask no.	Defining	Aligns to
1	Initial alignment marks and p-type areas	–
2	High dose n-type areas	1
3	Contact holes	1
4	Conducting paths and wire bonding pads	3
5	Electrical separation and anodical bonding areas	4
6	Optical slit	1
7	Pyrex cavities and anodical bonding areas	6

Table 4.1: Mask set overview where the first five mask concerns the SOI wafer processing and the last two the Pyrex wafer.

Structures enabling optimisation of the multiple photolithography steps are of outmost importance since they are the corner stones of the fabrication. Figure 4.1 shows the mask layout of positive and negative polarity resist test structures, which are present in all seven masks.



(a) (b)

Figure 4.1: Two polarities of resist test structures where the gray area is the chromium part of the mask and the triangle defines the optimum. Picture *(a)* shows a test structure for positive lithography and picture *(b)* a negative structure.

The resist test structures have been designed to easy distinguish between an over- or under-exposed wafer to find optimal exposure time followed by optimal development time. The triangle in the resist test defines the optimal situation, whereas an over-exposed/under-developed wafer will result in the lines below the triangle not overlapping (in the case of figure 4.1*(a)*, the reverse is true for picture *(b)*). Reversely, if the lines above the triangle are merging, the wafer is underexposed but not necessarily under-developed – which normally will appear as a coloured residual where there should be no resist. By having increasing overlap/gap between the lines the degree of over/under-exposure can be estimated. The line opposite the triangle is 5μm wide and 25μm long.

(a) (b) (c)

Figure 4.2: Mask layout of alignment marks. Picture *(a)* shows the resulting structure on the wafer, which the mask structure in picture *(b)* is align to to obtain picture *(c)*.

Another fundamental important structure is the alignment marks which have been designed to yield both coarse and fine alignment. Figure 4.2 shows the chosen layout. The small middle squares in figure 4.2.*a* have a side length of 5μm for fine alignment, whereas the large squares have a side length of 30μm. The blue part shown alone in figure 4.2.*b* constitutes the part of the mask that is transparent (dark field mask), which means that *(a)* is observed through *(b)* to obtain *(c)*. The most severe requirement for alignment is the alignment of the conducting paths to the contact holes of the digital sensor, where the tolerances are 1.5μm, which can and were obtained with the selected alignment marks.

From section 3.2.3 it became clear that the concentration level of the active areas are important for performance issues. Secondary Ion Mass Spectrometry (SIMS) was to be used to determine the actual dopant concentration to verify and better explain the results discussed in section 6.3. The SIMS measuring technique is a destructive process that sputters the sample surface using an ion beam. The sputtered atom that are ionised are then collected and mass analysed to obtain the dopant profile of the sample. Two of these SIMS test areas exists on the wafer, each on opposite sides of the centre. The SMIS test structure consists of an area of 1000μm by 2000μm, constituted by two squares with a side length of 900μm, where one have been doped with to the low energy BF_2 and the other with P. The actual SIMS analysis has not yet been performed, but is expected with great interest due to the amount of information contained in knowing the actual doping profile.

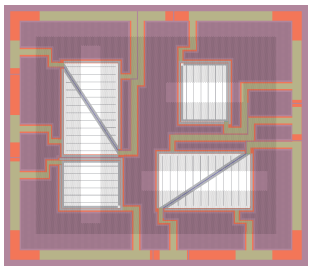


Figure 4.3: Layout of the seven superimposed masks for the analog device with contact fingers.

The mask design resulted in the layout shown in figure 4.3 where the seven masks are shown superimposed. In the following process section it is a good idea to keep the general mask layout in mind to better comprehend the various references to structures and actual fabrication pictures.

4.2 Process Sequence

This section describes the process sequence of the SOI wafer followed by the processing of the Pyrex wafer. This is only a narrative chronology since the two parts easily can be processed in parallel. The SOI wafer is processed through 59 main process steps involving 5 masks. Through these steps a device consisting of six separate pn junctions equipped with an optical filter and metal connections are constructed.

Ion implantation being the first main step and the most critical for the resulting efficiency, requires the growth and structuring of a 100nm thermal oxide layer in advance, since the implantation leaves no visual structures for further alignment. Creating the pn junctions is done by implanting B into specific areas of the n-type (P doped) device layer of the SOI substrate. This is carried out at a moderate energy (30keV), thus creating a junction depth, that ensures higher efficiency at short wave lengths and further more keeps the carrier life time low. The ohmic n-type contact is improved by further implant of a high dose of P.

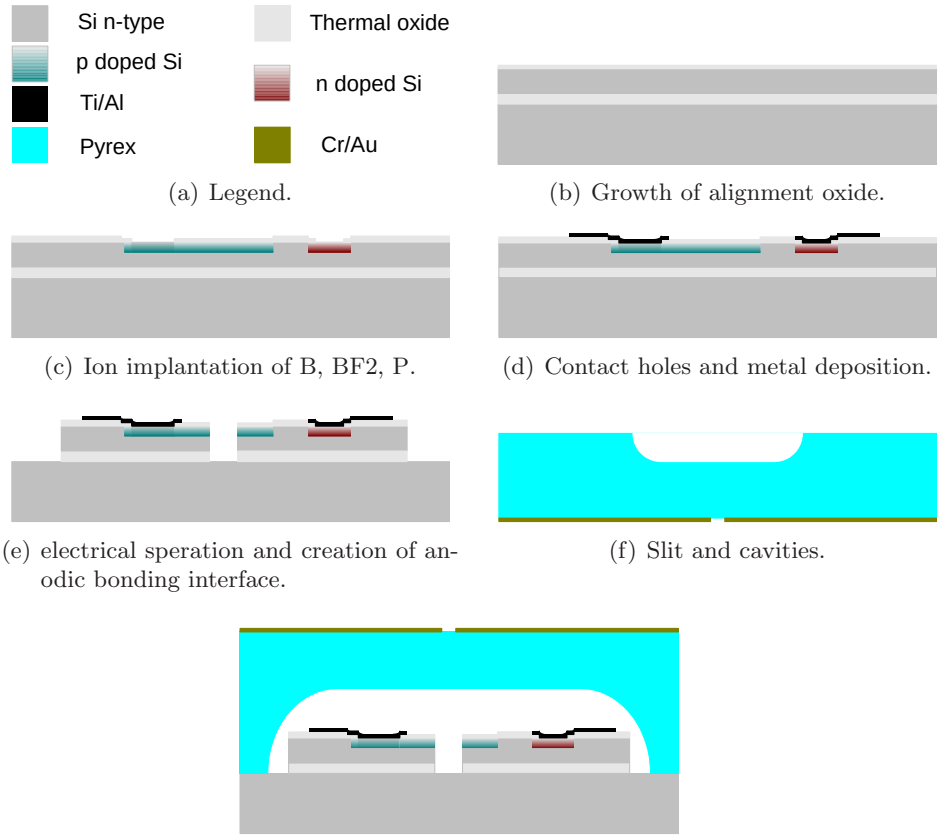
Two concentration levels of B is implanted to optimise the efficiency of the photodiodes. A high dose B is implanted with a very low energy (10keV) to ensure that a higher concentration resides in the upper part of the p well below the contacts. This enables good ohmic contact without a dramatic reduction of the carrier lifetime. The available ion implanter is due to mechanical constraints not able to deliver energies lower than 30keV. By implanting BF_2 at this energy the collision at the surface of the wafer will transfer energy to the Flour atoms of the splitting molecule, leaving the Boron atoms with an energy of approximately 10keV [15]. The structuring to obtain these two concentration levels at the specific areas is created by combining mask no. 2 and no. 3 in a negative photolithographic process. The first exposure in this process is done through mask no.2 followed by re-

versal bake and finally flood exposing through mask no. 3 – see appendix A step 8 and appendix B for mask layout. Section 3.2.3 derives the concentration levels and implantation energies used in the above described processes. Furthermore section 3.2.3 shows the simulated effect of the decisions made regarding the pn-junctions.

After the three implantation procedures the anti reflective oxide layer, also acting as a passivation layer, is grown. The design properties and details are described in section 3.2.4.

Next, the electrical contact to the active areas are established by opening holes in the oxide followed by e-beam evaporation of 15nm Ti and 200nm Al to create contacts, conducting paths, and wire bonding pads simultaneously. The Ti layer acts both as a diffusion barrier between the Al and Si especially during the anodic bonding (where the temperature reaches 350°C) and to increase adhesiveness of Al to Ti.

Finally the device areas and the individual sensors are electrically separated by etching through the device and buried oxide layers, leaving the



(a) Legend.

(b) Growth of alignment oxide.

(c) Ion implantation of B, BF2, P.

(d) Contact holes and metal deposition.

(e) electrical speration and creation of anodic bonding interface.

(f) Slit and cavities.

(g) Anodical bonded device.

Figure 4.4: Graphical overview of the entire process sequence.

bulk silicon to constitute mechanical support and anodical bonding interface. Etching through these three layers (oxide–silicon–oxide) is accomplished by a combination of wet and dry etching further described in 4.2.1.

The Pyrex part is fabricated through 24 steps using 2 masks resulting in a wafer processes on both sides constituting anodic bonding interfaces aligned to the optical slit. The latter is created first and consists of a 15nm Cr and 200nm Au layer, where – as in the case with the conducting path of the SOI wafer – the Cr layer increases adhesion.

As described in section 3.2.1 the Pyrex cavities are etched using a process further treated in section 4.2.1. The order of processing is due to alignment reasons, since it is easier to carry out the back side alignment to the metal structure of the slit than to the lower tolerance of the wet etched structures. Obtaining a good slit definition requires the deposition of an Al layer prior to the photolithography to prevent internal reflection of the UV light in the Pyrex.

Finally the two wafers are anodically bonded at a temperature of 350°C at 700V resulting in the bonded wafer pair shown in figure 4.5. A Si wafer with 160Å oxide is placed between the Pyrex wafer and the electrode during bonding to prevent diffusion of the Au into the electrode. After successful bonding the wafer is diced and access to the wire bonding pads is created; these two procedures are further described in section 4.2.3.

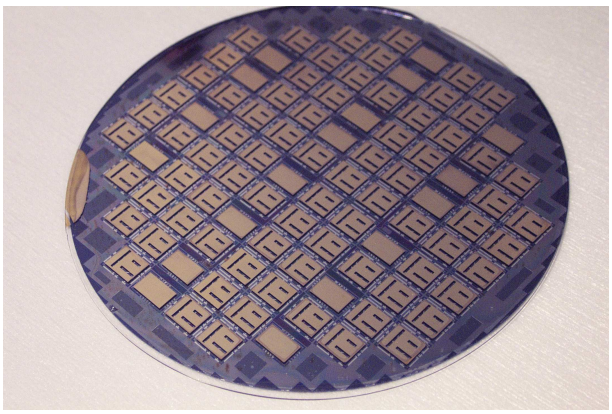


Figure 4.5: First completely processed and bonded wafer pair.

4.2.1 Selecting Etching Method

To promote the fabrication of a successful device, both with respect to performance and time constraints, process design was kept within well proven micro technological and in-house processing procedures. Optimisation of various photolithographic processes, metal deposition, and general cleaning is therefore not treated besides the details found in the process sequence in

appendix A. However one of the challenging elements was the design and optimisation of various etching procedures. Considerations and fabrication choices regarding these procedures are described and justified in this section. The process sequence consists of the following steps where etching is involved:

- First alignment mark - 100nm thermal oxide.
- Contact holes - 100nm thermal oxide.
- First step of the electrical separation - 100nm thermal oxide.
- Second step of the electrical separation - 5000nm monocrystalline silicon.
- Third step of the electrical separation - 1000nm thermal oxide.
- Pyrex cavities - 100nm Cr.
- Pyrex cavities - 11000nm Pyrex.

At the given facility Reactive Ion Etching (RIE) and general wet etching exists as two different ways of etching oxide and silicon. Where different properties can be obtained, such as the degree of isotropic profiles and material selectivity. Besides the difference in properties another reason for choosing one over the other is issues like contamination and batch processing. Due to cross contamination from the free sodium ions in Pyrex it is prohibited to process these wafers in the RIE clusters available. Hence the only option left is dedicated wet processing.

SOI Wafer

The first three bullets concerns the removal of 100nm of thermal oxide. This is done using 5 % buffered hydrofluoric acid (BHF) since the resulting under etch is not a problem due the thickness of the oxide versus the smallest tolerance between contacts and contact holes (1.5μm). Standard 1.5μm photo resist is used as masking layer – except for the layer in the electrical separation process which is treated in the following.

Etching through the device layer silicon is carried out with RIE using the recipe shown in table 4.2 resulting in vertical sides due to the anisotropic nature of the etch. Uniformity problems were encountered during this step appearing as a change in colour over the wafer. Profile measurements showed a difference of one 1μm from the centre to the perimeter of the wafer.

Recipe	SF_2 Flow	O_2 Flow	Pressure	RF power
OH_POLYA	32 sccm	8 sccm	80 mTorr	30W

Table 4.2: Recipe parameters for RIE of Si.

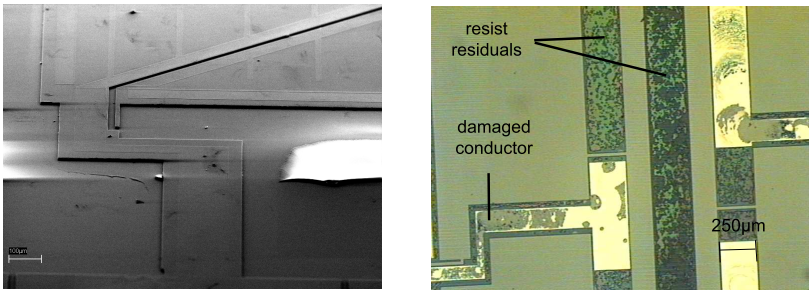
The phenomenon is ascribed macro loading effects and to the slightly higher flow of process gasses around the edge of the wafer, which increases both the chemical and the physical ion assisted etching. Total etching time of the device silicon was approximately 18 minutes compared to the expected time of around 12 minutes, which is based on the equipments nominal etching rate. The exaggerated etching time is depending on the etching area (loading effect) of the actual wafer and due to the fact that the buried oxide can be used as an etch stop, since the shown recipe have a selectivity of 20 between Si and oxide. It is thereby ensured that all the silicon is removed in the desired areas and that the vertical side walls are kept. A more direct approach to solve this issue is to use an end point detector (EPD) that shows the composition of the exhaust gas, thereby indicating when the bulk oxide layer is reached. However the EPD in the cluster system used was not reliable, hence the use of the method described.

Recipe	CHF_3 Flow	Pressure	RF power
MPSIO2	85 sccm	60 mTorr	200W

Table 4.3: Recipe parameters for RIE of SiO_2.

In validating the process sequence the first approach to etch through the bulk oxide was carried out using RIE. Table 4.3 shows the recipe used, which has a higher oxide etch rate compared to the OH_POLYA recipe in table 4.2.

In retrospect the choice of the recipe seems at best odd. Using only CHF_3 without adding CF_4 results in lower etch rates along with higher isotropy due to the lower creation rate of protective polymer, according to [17]. Due to the high RF power in the recipe the selectivity towards photo resist is low, however a resist thickness of 2.6μm was found to be sufficient for the 20 minutes of processing. Again the issues of conformity arose, but even



(a) (b)

Figure 4.6: The device after the electrical separation step. Picture *(a)* shows a SEM picture of an active area after the electrical separation through multiple etch processes. Picture *(b)* shows the damaged on the conducting paths frmo the RIE processes.

worse the resist seemed to be even harder burned resulting in extensive post cleaning when striping the resist. This fact along with the time consuming nature of RIE clusters suggested the use of BHF. It is however necessary to burn (20min at 250°C) the resist prior to the BHF-RIE-BHF process, which still leaves the problem of stripping the resist where a pure oxygen plasma was used to strip the resist.

Figure 4.6.b shows a microscope picture of a SOI wafer gone through all the steps of the SOI process sequence. It is clearly seen the the metal of the conducting paths have been damaged during the BHF-RIE-BHF process. A solution or a mitigating procedure have not yet been developed to deal with this problem, since the wafer used for the actual flight sensors was only effected in minor degree by this problem but had a high enough yield rated to provide the needed numbers of sensors. A possible solution is to optimise the oxide etch using RIE instead of BHF since the latter method is suspected to initiate the damaged shown in figure 4.6.b. Based on [17] it has been shown in [12] that it is possible to etch through 0.7μm oxide followed by 5μm device silicon and finally 0.5μm buried oxide using a resist thickness of 6.2μm employing the RIE recipe shown in table 4.4 as oxide etch.

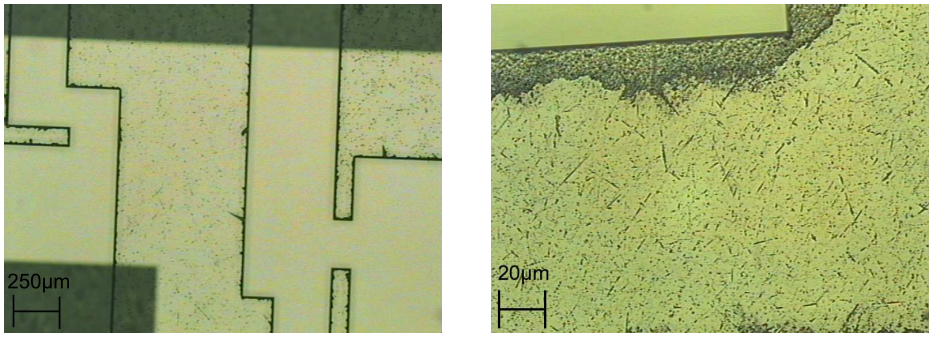
Recipe	CF_3 Flow	CHF_3 Flow	Pressure	RF power
JHHOX2	16 sccm	24 sccm	80 mTorr	100W

Table 4.4: Alternative recipe parameters for RIE of SiO_2

The recipe in table 4.4 is optimised with regards to a different loading and with respect to obtaining a high degree of anisotropy, which is not an issue in this case. Another improvement would be to use wafers with a buried oxide of only 0.5μm, which is still sufficient to ensure electric separation yet greatly reducing RIE process time. Figure 4.6.a shows one of the active areas after electrical separation process.

Pyrex Wafer

Wet etching is the only available solution to create the 11μm deep Pyrex cavities due to the cross contamination effects mentioned earlier. Concentrated 40% HF acid – resulting in an etch rate of 3.6μm/min – was used to etch the cavities thus placing severe requirements on the masking material owing to the extremely volatile nature of this acid. The front side of the wafer containing the slit was covered by a highly corrosive resistant adhesive polymeer (Blue Tape). Finding and optimising the proper masking material for the cavity side was very time consuming, as appendix I indicates. 100nm sputtered poly-Si and 4.2μm baked (5min at 90°C) resist was employed as a first approach – adapted from a method for creating fluid channels in Pyrex [1] – to find a suitable masking material. Subsequent anodical bonding tests proved difficult due to pinholes in the pyrex bonding interface arising from



(a) (b)

Figure 4.7: Pyrex anodic bonding interface with pinholes.

the interface being exposed to HF which have penetrated the masking layers. This pinhole effect is shown in figure 4.7.

A second approach utilised a 10nm Cr and 80nm Au layer instead of the poly-Si layer. This method however did not solve the pinhole problem but only added to process complexity. Especially the Au etch proved challenging due to a relative high etch rate of the iodine solution (KI, I_2, H_2O) used compared to the thin Au layer.

Finally a more simple solution was discovered consisting of only a 100nm Cr layer along with hard baked (5min at 120°C) 4.2μm resist. As in the second approach the Cr is etched using a solution of Cerium sulfate, HNO_3 and H_2O. This procedure successfully resulted in an anodic bonding interface without any pinholes depicted in figure 4.8. A conformity difference of 0.2μm was measured from the centre of the wafer to the edge, which is not considered a problem with respect to the subsequent bonding – due to the clamping of the wafers during the bonding procedure.

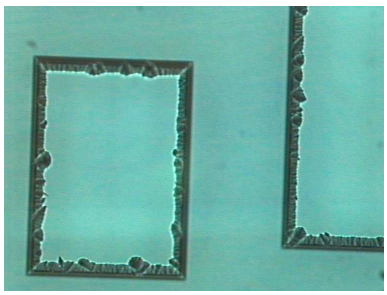


Figure 4.8: Interface without pinholes. The small square is 500μm wide. This picture is take with a microscope different from the other pictures, hence the colour difference.

4.2.2 Alignment Issues

During fabrication a few challenging alignment issues arose despite efforts made during the design phase to ensure optimal alignment. First the two

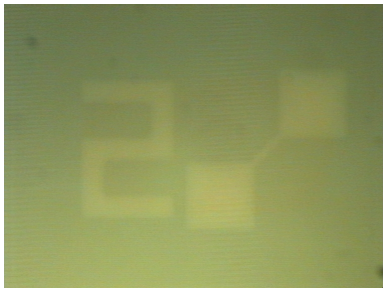
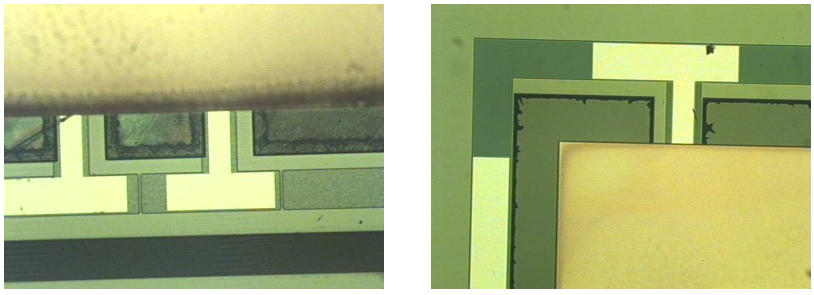


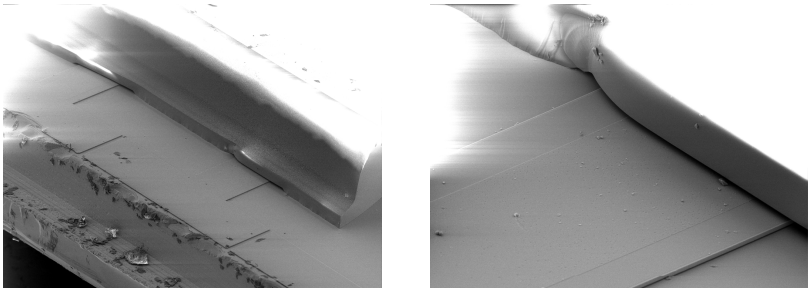
Figure 4.9: Alignment mark after the second thermal oxide have been grown

oxidation steps were considered to create alignment problems, but could easily be solved by growing a thicker oxide in the very first process step. However, as the microscope picture in figure 4.9 shows it was not necessary to grow an oxide thicker than 100nm. It can been seen from the mask design described in section 4.1 that alignment marks for the alignment of the Pyrex and the SOI wafer are incorporated in the design with a tolerance of 45μm. It turned out however that the optical alignment equipment for the anodical bonder was not functioning properly, leaving the alignment to be done by hand held visual inspection. This method is not normally associated with micro technology but in the current situation it was to some degree successful which can be seen from figure 4.10. Despite the misalignment shown in figure 4.10.*a* the structure is still bonded due to the sloping side walls of the Pyrex ensuring no contact between the conducting path and the bonding interface. The sloping side walls also contributes with a degree of self aligning where the two wafers are forced into place due to the structuring. This effect can easily be detected when manually adjusting the wafers prior to bonding, which greatly improves the the aligning procedure. A side view of the interface is shown in figure 4.11 where it is seen that the Pyrex cavities successfully encompasses the conducting paths as designed.



(a) (b)

Figure 4.10: Result of manual alignment prior to anodic bonding. Picture *(a)* shows a slightly more misaligned bonding than picture *(b)*, which shows the highest achieved manual aligning.



(a) (b)

Figure 4.11: SEM picture of the anodic bonding interface. Picture *(a)* shows two bonding pads with conducting paths going beneath the Pyrex cavity. A closeup of the interface is shown in picture *(b)*.

4.2.3 Wafer Dicing and Pyrex Ledge Separation

Figure 4.12 depicts how the wafer stack is diced. Three lines are cut in the bonded wafer pair; Lines no. 1 and 2 are 400μm deep and line no.3 dices the chips. Parts A and B are subsequently removed by applying a controlled pressure on the parts using the Pyrex Ledge Separation Tool (PLST). This tool was specially designed for applying a mechanical pressure by controlling the vertical movements of a thin steel blade, which could be manually aligned with the Pyrex saw lines. The SEM pictures in figure 4.13 shows the condition of the chip prior and post to the ledge separation. Concerns regarding the PLST technique arose since the Pyrex ledge can only be moved 5μm before colliding with the conducting paths beneath, thus suggesting that the ledge would not dislodge. However picture *(b)* in figure 4.13 discarded these concerns, where it is clearly seen the the Pyrex ledge is cleanly removed to expose the underlying wire bonding pads. In a few cases the pressure applied by the PLST was too great or even not aligned with the cut resulting in destruction of the conducting paths or even cleaving the chip. However a general yield rate of 90% was achieved with the PLST. It is also clearly seen from the picture *(b)* that the cutting depth of the saw

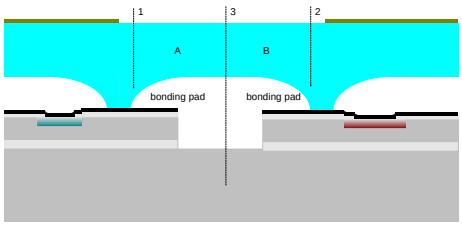
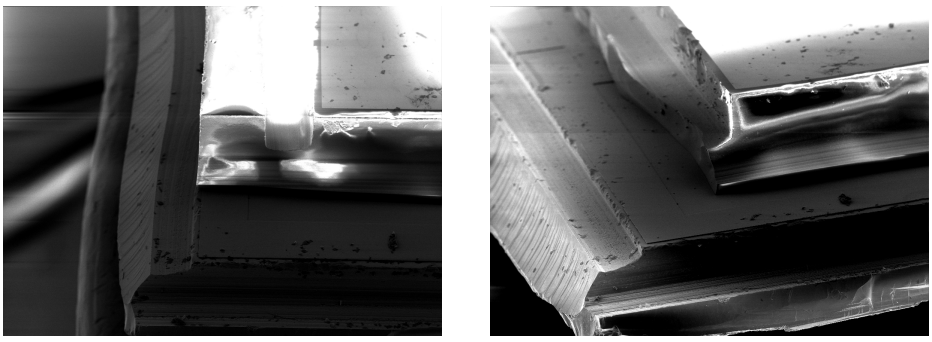


Figure 4.12: Dicing method where part A and B are the Pyrex pieces to be removed after the wafer stack have been diced in the order indicated by the enumerated sawing lines.

is not consistent since the two cuts in the bulk Si should have been at the same level. This difference is ascribed in part to the general condition of the 20 year old saw, but mainly to irregularities in the Blue Tape applied on the backside of the wafer stack to keep the chips together once diced.

A high risk of physical contamination exist during the dicing procedure due to the possibility of transferring Si/Pyrex sawing dust with the inherent cutting water. Therefore the wafers are continuously flooded with DI-water from an external source in an attempt to prevent sedimentation of the dust on the active areas. Access to the interior of the sensor, as seen in figure 4.11 *(b)*, is limited to a small channel around each conducting path leading from the wire bonding pads. Thus the in flux of particles is expected to be very limited. The magnitude of these contamination issues are not thoroughly investigated, but visual inspection after dicing showed some signs of residuals. Resulting degradation of the output signal have however not been directly associated.

Dicing the wafers could altogether be avoided by employing so called interconnects and separating the chips by using the ASE tool (which is a Deep RIE equipment that became available after the actual processing had ended). Interconnects routes contact to the backside of the SOI wafer thus the chips could be soldered directly to a substrate or PCB without the need of fragile wire bonds. Interconnects has e.g. been studied by Heschel [16].



(a) (b)

Figure 4.13: Dicing and ledge seperation. Picture *(a)* show a chip after dicing and *(b)* shows the same chip after the ledge separation procedure.

5

Electronics Design & Mechanical Integration

The chapter gives an overview of the designed and fabricated driver circuit for the sensor chip, and describes how the five sensors are placed and connected in the satellite. It also set focus on the scaling factor associated with the change from earth based measurement to actual in-orbit conditions. Finally the mechanical layout and integration are also briefly described.

5.1 Electronics Design

Electronic circuit designed through three iterations.

Design, validation and fabrication of the sensor driver electronics was conducted in parallel with the chip development. First a two-layer Printed Circuit Board (PCB) principle validation model was made, then a four-layer engineering model, and then finally the four-layer flight model presented in this chapter.

The constraints and requirements from the different satellite subsystems governed the design of the circuit, where especially the available 3.3V regulated voltage gave rise to extra considerations when selecting the different components.

The main purpose of the circuit is to amplify the sensor signal through a current to voltage conversion using an operational amplifier (OPAMP) setup, and subsequently carry out the division of the converted triangular current difference signal ΔI_t with the reference signal I_{ref} in order to obtain the linear characteristic along with the elimination of undesired parameters described in section 2.1. As the schematic in figure 5.1 shows, ΔI_t is obtained by connecting the two triangular sensor areas in parallel with opposite orientation. This connection methods promotes noise tolerance since the resulting current loop mitigates diode leakage and the associated resulting output voltage offset. Furthermore the Common Mode Rejection

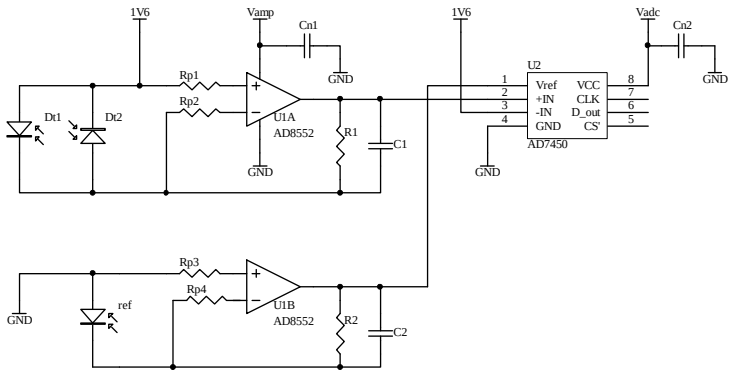


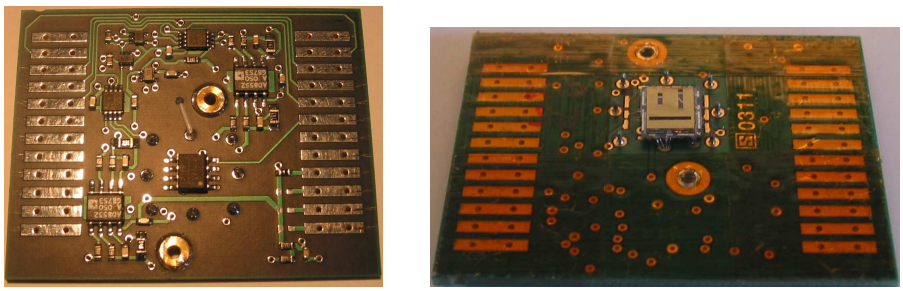
Figure 5.1: Circuit schematic of one side of the sensor. The upper OPAMP is connected to the triangular sensor areas and the lower converts the sensor reference area current to a voltage driving the reference input of the A/D converter.

(CMR) of coupled noise is ensured by the impedance (R_p) connected to the OPAMP. The voltage reference placed at 1.6V centres the OPAMP output voltage at this value for a 0° angle of incidence.

Division of signals carried out by a single A/D converter.

The actual division of the signals is realised using a true bipolar and fully differential analog input A/D converter (AD745B) where the reference input V_{ref} determines the span of the converter and thereby acts as a divider. V_{ref} is generated by the current to voltage conversion of the output from the reference area on the chip – schematically shown at OPAMP U1B in figure 5.1. The different passive component values have been determined from common circuit analysis and are considered outside the scope of this report except for the description of the how the scaling factor is found which influences the values of R1-4 (section 5.2). A validation of this division principle is given in section 6.1.

A sun detection circuit is included to determine whether the present sensor is illuminated by direct sun light or not. This is done to avoid a situation where small signals are divided, which could lead to a false angle



(a) Front (b) Back

Figure 5.2: Picture of the front and backside of the resulting flight PCB.

measurement. This sun detection circuit is realised by employing a bilateral switch which activates the A/D converter if both sensor reference signals are above a predefined threshold.

Load	Active Current	Standby/Quiescent Current
Two A/D converters	1600μA	6μA
Two OPAMPs	2000μA	0μA
Two NAND gates	3400μA	40μA
Bilateral switch	1700μA	20μA
Temperature sensor	1500μA	1μA
Total	10.2mA	67μA

Table 5.1: Power budget for a single sun sensor PCB.

The sun sensor PCB also includes a temperature sensor placed directly on the opposite side of the chip. The sensor uses a standard one-wire technology, which only requires an operating voltage and gives the temperature as a digital output on the same line as on which it is addressed. The temperature sensor is employed mainly to evaluate if the thermal considerations and conclusions regarding the entire satellite, but the measurements are also valuable when interpreting the sun sensor data.

The PCB is powered down when measurements are not required.

As seen from figure 5.1 V_{adc} and V_{amp} uses the same 3.3V regulated voltage, but is divided into two separate connections in order to save power, since the Serial Peripheral Interface (SPI) bus employed does not tolerate a floating signal from the A/D converters if these were to be turned off. As a result only the V_{amp} lines are turned off when the system is not used, which is power-wise reasonable since the A/D converters automatically goes into a standby mode when not used. The estimated power consumption of a single sun sensor PCB is shown in table 5.1.

The resulting PCB is seen in figure 5.2 where the 12 pin flat cable interface to the main ACDS board also is seen at the perimeter of the board.

Pin	Function	Value
1	`sun detector`	analog out
2	`SPI CS2`	active high
3	`SPI CS1`	active high
4	`SPI CLK`	clock signal
5	`SPI data`	-2048 to 2047
6	`temp`	one-wire digital bus
7	`Vadc`	3.3V (regulated)
8	`GND`	ground
9 - 12	`Vamp`	3.3V (regulated)

Table 5.2: I/O connections.

Five of these PCB's were placed on different sides of the satellite, where the last side (the payload side) was not covered due to mechanical constraints from the tether and camera housings. Four of the five PCBs are connected in a chain to the same flat cable and share all connections. The individual PCB is selected through the four V_{amp} lines where the relevant board is activated by preset jumpers on the sensor PCB. This addressing scheme is controlled by the OBC via the main ACDS board. The pin connection of the interface is described in table 5.2.

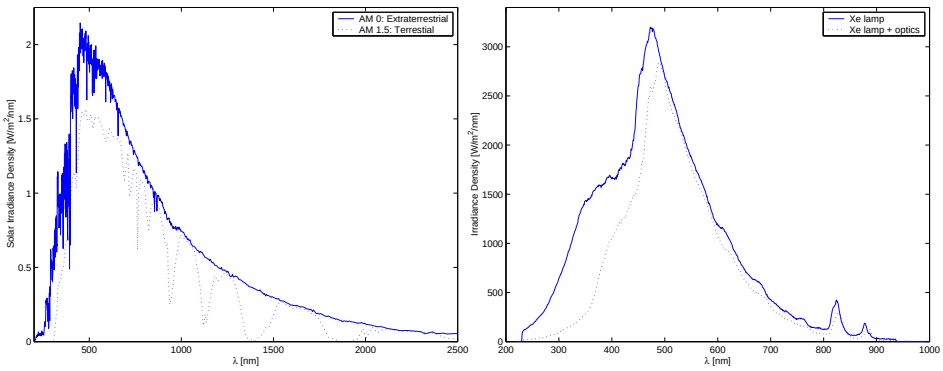
The four-layered PCB yields high noise immunity.

The bottom layer and layer two of the PCB are ground planes, and with signals routed in layer three the PCB should be very noise tolerant. Furthermore ground plates are added under critical components in the top layer. Digital lines have also been avoided under critical components to enhance noise reduction. Appendix C can be consulted for further details on the sun sensor circuit and PCB layout.

5.2 Generated Currents in Orbit – Scale Factor

The generated photocurrents in orbit must be estimated to avoid saturating the OPAMPs in the driver electronics. Figure 5.3 shows the solar spectrum [33] and the spectrum for the used xenon lamp in the setup described in section 6.1.1. The lamp spectrum was measured at MIC, and the shown spectra are the measured minus the dark current spectrum of the analyzer. Note, that the amplitudes of the spectra are not to scale since this was not possible with the analyzer. However, the indication that the amplitude for the lamp with subsequent optics is lower than for just the lamp is naturally true.

The generated currents in orbit is found by integrating the product of



(a) (b)

Figure 5.3: *(a)* Solar spectral irradiance curves for air mass 0/space (AM0) and AM1.5/Earth. *(b)* Spectral irradiance for a xenon lamp and a xenon lamp and subsequent optics (amplitudes not to scale).

the spectral sensitivity $S(\lambda)$ [A/(W/m^2)] of the sensor and the solar spectral irradiance distribution $D(\lambda)$ [(W/m^2)/nm] over all wave lengths:

$$I_{orbit} = \int S(\lambda)D(\lambda)\,\mathrm{d}\lambda \tag{5.1}$$

However, since the sensitivity of the sensor was not known at the time of satellite integration this method cannot be used. After integration the quantum efficiency was measured, but the obtained results cannot be used either; cf. section 6.2. Therefore the method described in the following has been used instead.

Table 5.3 shows the optical power in the wave length range 450-1020nm measured with a HP 8152A Optical Power Meter for different distances between the xenon lamp and the sensor position and outdoors on a cloud-free summer day (∼AM1.5). The generated currents in a photodiode on the sensor are also shown.

Description	**Optical Power**	I_{photo}	**Scale Factor**	$I_{photo,space}$
Optics lab (78.7cm)	$203.21\frac{\mathrm{W}}{\mathrm{m}^2}$	18.85μA	2.37	44.7μA
Optics lab (88.9cm)	$148.71\frac{\mathrm{W}}{\mathrm{m}^2}$	15.43μA	3.24	49.7μA
Optics lab (111.8cm)	$86.07\frac{\mathrm{W}}{\mathrm{m}^2}$	9.72μA	5.59	54.4μA
Outdoors	$611.16\frac{\mathrm{W}}{\mathrm{m}^2}$	47μA	1.45	68.06μA

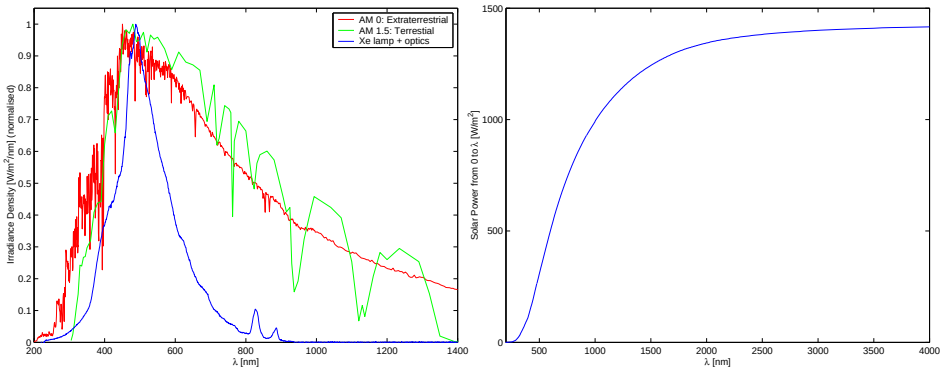
Table 5.3: Measured optical power in 450-1020nm, measured photocurrents, scale factors, and expected currents in space. Note that the chip used for measurements outdoors is not the same as the one used in the optics lab.

A scale factor (SF) to scale the currents to the expected currents in space can be found by evaluating the spectra from figure 5.3. Figure 5.4(a) shows normalised versions of the solar and lamp spectra. The scale factor is given by the ratio of the sun power in orbit (cf. 5.4(b)) and the optical power exposed to the sensor during testing[1]. However since the sensor is mainly exposed to optical power in 350-650nm with the xenon lamp we use:

$$SF = \frac{P_{AM0,350\mathrm{nm}-650\mathrm{nm}}}{\frac{P_{Xe+optic,450\mathrm{nm}-1020\mathrm{nm}}}{\int_{450\mathrm{nm}}^{1020\mathrm{nm}} D_{Xe+optic}\,\mathrm{d}\lambda}\int_{350\mathrm{nm}}^{650\mathrm{nm}} D_{Xe+optic}\,\mathrm{d}\lambda} \tag{5.2}$$

However, this method does not account of currents generated outside 350nm-650nm, but as shown in section 6.2 the sensor has most of its sensitivity in this region, which then implies that the SF approximation is not that bad. Table 5.3 shows the resulting SFs for the three laboratory measurements. These SFs does not lead to the same expected currents in orbit.

[1] Optical power is given in power per square meter.



(a) (b)

Figure 5.4: *(a)* Normalised spectrums for lamp+optics, AM0, and AM1.5. *(b)* Solar power from 0nm to λ (AM0).

Ideally if the xenon light beam was completely collimated and uniform then the optical power measurements would yield the same result for all distances. A high degree of collimation was desired for performance evaluation, which was to some degree achieved at the expense of uniformity. Since the expected current grows with the measuring distance other error sources may be present in addition to non-uniformity – the trend in table 5.3 indicates that lack of collimation must play a central role in explaining the differences in the power measurements. Back-estimating from the optical measurement starting at 450nm to 350nm is naturally also a problem with the method, but as shown in figure 5.4(a) the curves are not that different in shape at 350-450nm.

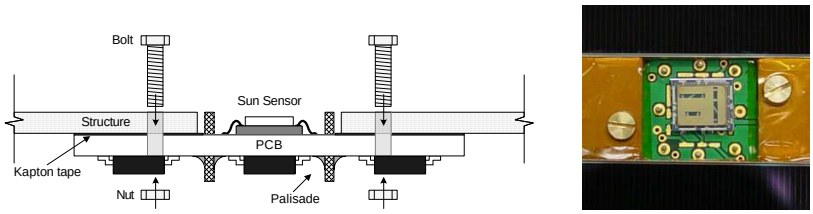
Measurements performed on a sunny day with the sun as a simulator for the sun in space are also given in table 5.3. The method for finding the scale factor is equivalent:

$$SF = \frac{P_{AM0,350\text{nm}-650\text{nm}}}{\frac{P_{earth,450\text{nm}-1020\text{nm}}}{\int_{450\text{nm}}^{1020\text{nm}} D_{AM1.5}\,\mathrm{d}\lambda} \int_{350\text{nm}}^{650\text{nm}} D_{AM1.5}\,\mathrm{d}\lambda} \tag{5.3}$$

The outdoor measurement is the most trustworthy. By using a scale factor of two to scale current peaks measured outdoors saturation should be avoided. Actually this scale factor of two was also used for the Ørsted satellite [4].

5.3 Mechanical Integration

On DTUsat the sun sensor is integrated with the mechanical structure as illustrated in figure 5.5. The sensor chip is glued directly to the PCB containing the necessary measurement and interface electronics described in the previous section. Electrical contact between the chip and the gold-plated



(a) (b)

Figure 5.5: Mechanical integration of the sun senor PCB. Picture *(a)* shows how the sensor chip is mounted on the backside of a PCB having view through rectangular holes in the satellite's walls. Picture *(b)* shows the sensor mounted between the solar cells on DTUsat.

PCB is realised with direct wire bonding. To protect the wire bonds – especially during assembly of the satellite – the chip is surrounded with a palisade consisting of 8 pieces of component wire soldered to the PCB in the interior; the palisade was chosen since this solution was less time consuming than finding an encapsulation that also protects the wire bonds during thermal cycling.

The dimensions of the PCB is $3.9 \times 5\text{mm}^3$ and it has a mass of 7.1g including sensor chip, kapton tape, palisade, and nuts. Estimates yield that this can be lowered to below 3g if two layer PCBs and further component packing is employed; however this may increase the experienced noise. Table 5.4 show the total mass budget for the sun sensor system integrated on DTUsat.

Item	Mass
Five PCBs with chip, kapton tape, guard pins and nuts	35.5g
Interconnects	
One pieces of 1.5", 9 pins	1.1g
One pieces of 2", 12 pins	1.5g
Three pieces of 2", 12 pins	5.4g
Total	46.5g

Table 5.4: Mass budget for sun sensor PCBs and connections on DTUsat.

6

Performance Evaluation

The majority of the time on this project was spent on design, development, and fabrication of functioning sensors. The last part was very critical since the sensors had to be ready for integration on DTUsat prior to launch. However, to validate that the sensors are in fact functioning correctly various tests were naturally performed. In addition to these tests calibrations were performed to relate sensor measurements to a known coordinate system.

These tests and calibrations are described in this chapter. The testing phase is by no means completed, since this goes far beyond what is possible in this special course. More environmental tests like vacuum, shock, radiation, and thermal cycling are needed for space qualification. As explained in section 1.2 vacuum testing is currently being conducted at the University of Applied Sciences Aachen, Germany. Likewise it is our hope that the SSETI mission and future DTUsat missions will bring new results.

6.1 Evaluation of Sensor Principle

To validate the sensor principle sweeps with incoming light in the $[-70°; 70°]$ range was conducted. The first section below describes the hardware setup that was controlled with LabVIEW, and the proceeding section interprets the results.

The scheme described in the next section was actually also used to test the measuring principle before the sensors had been fabricated. This was carried out by simulating an ideal sun sensor with a MATLAB script that was called from LabVIEW, and by producing the current characteristics with a programable Keithley SourceMeter.

6.1.1 Test Setup

Figure 6.1 illustrates the general test setup used for testing the fabricated devices and table 6.1 lists the used equipment. If the setup is to be assembled

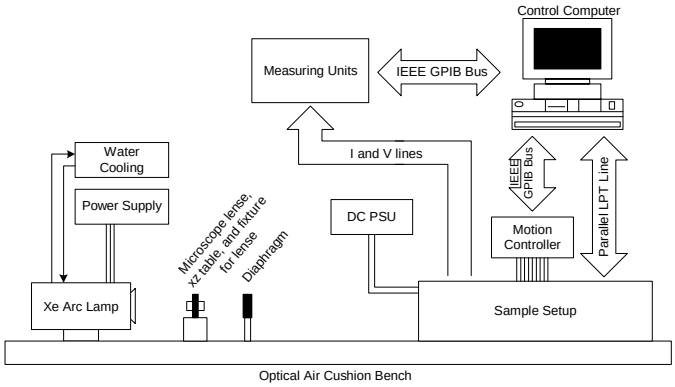


Figure 6.1: Overview of the test setup. The boxes *Sample Setup* and *Measuring Units* may vary from test to test.

again then the equipment in the list are located in various research groups at MIC and COM. The developed LabVIEW programs are included on the enclosed CD-ROM, and appendix E gives a short description of the most important programs.

The lense and diaphragm focuses and collimates the light beam from the xenon lamp; the spectrum of the lamp can be found in section 5.2. By using this setup the uniformity of the beam cannot be controlled. The non-uniformity has not been measured, but it is not so pronounced that it can be seen by visual inspection and it is not expected to be a problem since only a very small part of the beam is selected with the diaphragm. Better uniformity can be obtained by adding a subsequent lense-diaphragm step after the diaphragm, but doing so will lower the optical power significantly.

The sample to be measured is normally either a sensor chip where the currents are to be measured directly or a sensor chip mounted on a PCB where the ADC output is used. The currents or ADC output is sampled with repeated measurements in each point automatically with LabVIEW via multimeters connected via GPIB and by reading the ADCs directly from the COM port. When controlling the ADCs via the COM port Schmitt triggers should be used since the signals from the control PC are of a very low quality. In both cases the sample is rotated from $-70°$ to $70°$ in $0.1°$ steps.

Note: Variations of the Setup

- When measuring directly on a sensor chip the chip is held in place on a vacuum chuck and connections are made with contact needles.
- When performing tests with a chip mounted on a PCB the PCB is mounted on a custom made holder for the theta rotation stage.
- When simulating the chip currents with MATLAB and Keithley SourceMeters contact to the bonding areas on the PCB are made with spring

Position Related:
Newport Motion Controller MM3000
Newport URM80/100PE Theta Stage
Newport 850FV6 Actuator (2 units; xy table)
Thyra Control Computer[1]
Current/Voltage Sources:
HP E3611A DC Power Supply
Keithley 2000 Multimeter (2 units)
Keithley 2400/2410 SourceMeter (2 units)
Optics:
Oriel 60115 Xe Arc Lamp Lamp
Oriel 68806 Arc Lamp Power Supply
Coherent Solid-State Temperature Control T251P-2C
Standard diaphragm
Leitz Pl32x Microscope Lense
Micro Contrôle xz Table including fixture for Leitz lense
Other (needed for special made tools etc.):
Newport Optical Air Cushion Bench
Quater XYZ Table Model 300TR (2 items)
Vacuum chuck
Charles Austen Capex 2 Pump (for chuck)[2]

Table 6.1: Equipment used in the test setup.

loaded contact needles fixated in a custom made polycarbonate fixture.

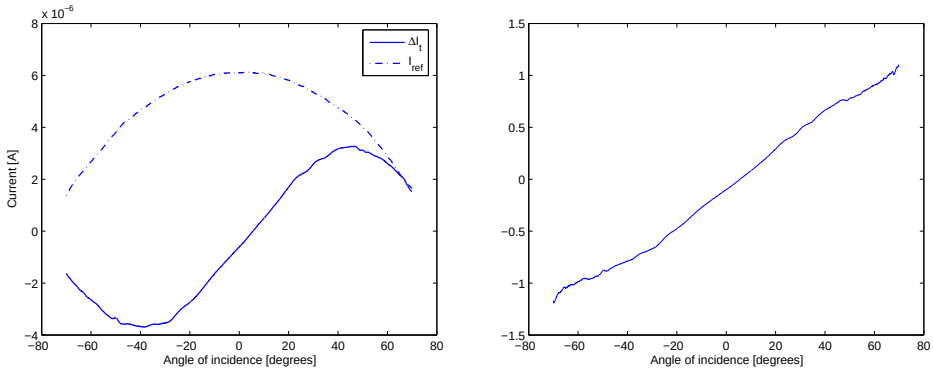
- When conducting calibration measurements on a half sphere the theta stage was mounted vertically on a custom made polycarbonate plate that can be rotated in the horisontal plane.

6.1.2 Evaluation of Measurements

Figure 6.2(a) shows measured ΔI_t and I_{ref} from a sensor chip. The amplitudes on these graphs are of course much lower than what is expected in space. The reason for this is the low power density from the used collimated xenon lamp. Calculations along with experiments have confirmed that the amplitude will be around the desired 100μA at 0°. With this amplitude correction the obtained results are close to the ones of the ideal device shown in figure 3.9(a).

[1] It is recommended *not* to change any settings on the computer related to the GPIB interface card! The card is not a National Instruments card, which results in great difficulties when configuring for use with LabVIEW.

[2] Simple old pump. Replacement might be a good idea.



(a) (b)

Figure 6.2: *(a)* Measured ΔI_t and I_{ref} currents from a sensor chip. *(b)* Calculated response from an ideal division.

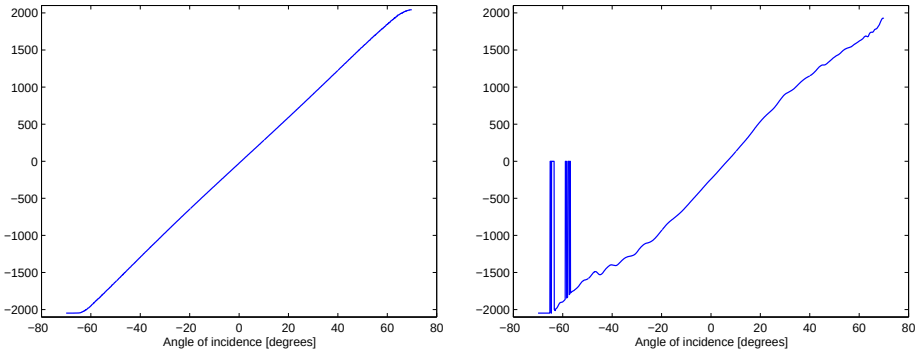
In figure 6.2(b) $\Delta I_t / I_{ref}$ has been calculated from the data in figure 6.2(a). This is not as linear as the ideal device which of course is due to imperfections in figure 6.2(a). At large angles the output is not single valued in some small regions which of course limits the obtainable resolution in these regions. This is due to the bumps seen in figure 6.2(a); investigations on these are to be conducted and hopefully removed in a second generation. An offset error is also present due to an offset in ΔI_t, which is due to differences in efficiency for the two triangles – however, it may also be partly due to non-uniformity of the xenon light beam. The device is of course still useable with these imperfections since interpolation or a look-up table can be used instead of some linear parameters.

Figure 6.3(a) shows a conversion performed by the used ADC. Instead of having sensors mounted on the PCB the currents of an ideal sun sensor was simulated by a MATLAB program in LabVIEW as described above. The output is seen to be very linear which validates the division implementation described in section 5.1. Some saturation due occur since the gain resistors were not optimised before performing the test.

An ADC conversion from pre-flight electronics and sun sensor is shown in figure 6.3(b); the zero outputs are due to start-up problems in the test setup and not to the electronics or sensor chip. The bumps are similar to the ones in figure 6.2(b) (but from a different sensor chip) and since the ADC conversion is very linear (cf. figure 6.3(a)) the reason for them is naturally identical.

The standard deviations for the characteristics in figure 6.2 is plotted in figure 6.4(a). Figure 6.4 plots standard deviations for the ADC outputs in figure 6.3. The deviation of zero above $\sim 60°$ is due to saturation during the experiment, and the peaks are due to the start-up problems in the test setup.

In the region $-50°$ to $50°$ the standard deviation in figure 6.4(b) (top)

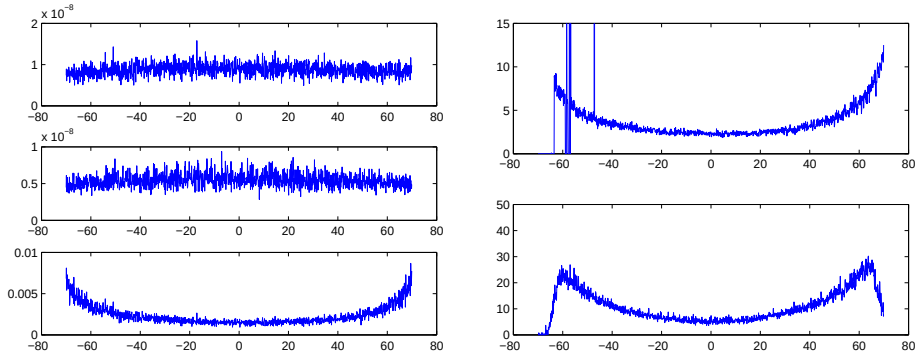


(a) (b)

Figure 6.3: ADC response from *(a)* a simulated ideal sun sensor, and *(b)* a sun sensor chip. The zero-outputs are due to problems in the start-up phase of the test.

is within 5 engineering units, which with the used 12bit ADC corresponds to errors $\leq 0.17°$. Figure 6.4(b) (bottom) shows higher deviations with the ideal sensor simulation which is ascribed to noise in the setup. The higher deviations for large angles is due to the low amplitudes of the reference signal.

Due to the short available testing period on DTUsat it has not yet been tested what performance that can actually be achieved in space. However, from the above example and the graphs it is clear that systems with a resolution of at least $1°$ should be feasible in the $-40°$ to $40°$ region. For larger angles it might be more difficult to achieve a resolution below $1°$ due to increased noise (due to decreasing I_{ref}) and the bumps in figure 6.2(b).

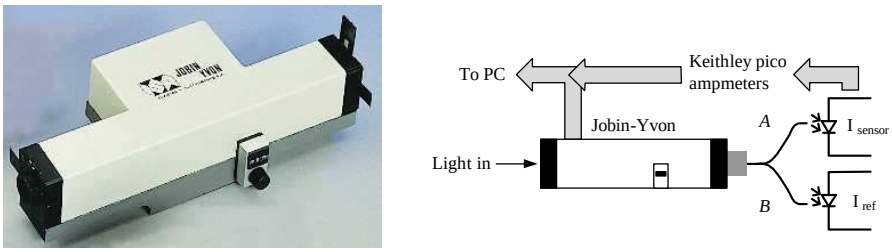


(a) (b)

Figure 6.4: *(a)* Standard deviations for ΔI_t, I_{ref}, and $\Delta I_t/I_{ref}$ for a sensor chip. Units: ampere for the first two, and the third is dimensionless. *(b)* Standard deviations for $\Delta I_t/I_{ref}\big|_{ADC,chip}$ and $\Delta I_t/I_{ref}\big|_{ADC}$ for an early validation test of pre-flight electronics and sensor and of the electronics with a simulated sensor. Units: engineering units of the ADC.

6.2 Quantum Efficiency

To validate that the sensor mainly has an output in the short wavelength (UV) regime it was tested with a monochromator. At MIC the only available monochromator is a Jobin-Yvon H20, which is operated manually. Since many measurements was wanted time was spend on automating it with a DC stepping motor controlled with a LabVIEW program that also carries out all the needed measurements – cf. appendix F.



(a) (b)

Figure 6.5: *(a)* Jobin-Yvon H20 monochromator. *(b)* Setup for measuring the quantum efficiency. The output fiber is bifurcated and ends in two arms. One arms ends in a ferrule connected to a reference diode (B), and the other ferrule is mechanically fixed to point at a sensor area (A).

The quantum efficiency was measured with the setup shown in figure 6.5(b). By measuring the dark currents for a reference diode and a photodiode on the sensor, and their currents for different wavelengths the quantum efficiency can be determined by:

$$QE_{DUT} = QE_{ref} \frac{I_{sensor} - I_{sensor,dark}}{I_{ref} - I_{ref,dark}} K \tag{6.1}$$

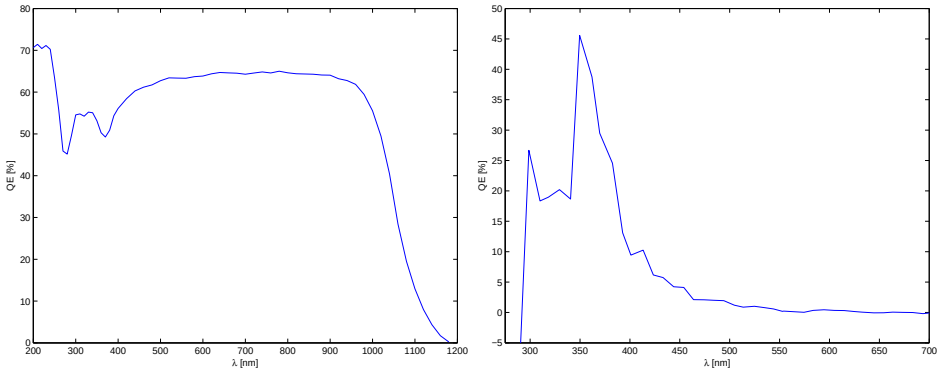
where QE_{ref} is the quantum efficiency for the reference diode shown in figure 6.6(a), and K accounts for the optical power distribution in the two arms of the bifurcated fiber with the relation $P_B = KP_A$. Linear interpolation is used to find QE_{ref} for wave lengths not present in the reference diode data.

Figure 6.6(b) shows the result of the measurements. From this it is seen that the sensor mainly has an UV response. However, further interpretation of the graph is not possible since some serious problems where present in the setup. Fixating the ferrule properly to a photodiode on the chip proved difficult, which means that the actual amplitudes of the quantum efficiency may be incorrect. Evaluation of the raw data files indicates that this is in fact true.

In addition to this there is a problem with the halogen light source, since it does not have much power below 350nm. This makes measurements in the UV regime more difficult. The leap in 6.6(b) around 340nm is due to the fact that the sensor only has a one layer anti-reflective coating and because the

diffraction index for Si changes here [19]. As suggested in section 3.2.4 the quantum efficiency could be improved by using another oxide thickness in the anti-reflective coating (cf. figure 3.17). That the quantum efficiency becomes negative in 6.6(b) clearly indicates that the measurements are not correct. Other technicalities also influences the results as explained in appendix F.

To gain more insight to the actual quantum efficiency the test setup should be improved, and more measurements should be conducted. However, for validation purposes the result can be used to show that we actually have a response in the short wave length regime. The measurements were carried out without the Pyrex lid. Pyrex is not transparent below 300nm, which means that the sun sensor has its main response in 300-450nm.



(a) (b)

Figure 6.6: Quantum efficiencies. *(a)* Reference photodiode. *(b)* Sun sensor area (Vertical ref. area chip 88.). The reader is strongly urged to read the text above to avoid over-interpretation.

Determining K

The power distribution factor has to be determined for a specific assembly of the light source, monochromator and fiber coupling. This was done by first making measurements for all desired wave lengths with the reference diode on A and a second diode allowing easy ferrule connection on B (cf. figure 6.5(b)). For this we have:

$$P_{A,1} = \frac{I_{ref,1}}{S_{ref}} \quad , \quad P_{B,1} = \frac{I_{2nd,1}}{S_{2nd}} \tag{6.2}$$

where S is the sensitivity [mA/W]. Secondly the two diodes are interchanged and the measurements are repeated, so that we have:

$$P_{A,2} = \frac{I_{2nd,2}}{S_{2nd}} \quad , \quad P_{B,2} = \frac{I_{ref,2}}{S_{ref}} \tag{6.3}$$

The quantum efficiency is proportional to the sensitivity through an energy relationship. Inserting (6.2) and (6.3) in $P_B = KP_A$ and using $QE \propto S$ gives:

$$K\frac{I_{ref,1}}{QE_{ref}} = \frac{I_{2nd,1}}{QE_{2nd}} \quad , \quad K\frac{I_{2nd,2}}{QE_{2nd}} = \frac{I_{ref,2}}{QE_{ref}} \tag{6.4}$$

Multiplying these relations and rearranging the result gives us an expression for the optical power distribution in the two arms:

$$K^2\frac{I_{ref,1}}{QE_{ref}}\frac{I_{2nd,2}}{QE_{2nd}} = \frac{I_{ref,2}}{QE_{ref}}\frac{I_{2nd,1}}{QE_{2nd}} \quad \Rightarrow$$
$$K = \sqrt{\frac{I_{ref,2}}{I_{ref,1}}\frac{I_{2nd,1}}{I_{2nd,2}}} \tag{6.5}$$

6.3 IV Characteristics

The IV characteristics of a few chips where measured in addition to the optical measurements. Results presented in the following resides from chips no. 21 and 71, which have no Pyrex lids.

The current I_d through a pn junction diode as a function of the voltage V_d is described by:

$$I_d = I_s\left(e^{\frac{V_d}{nV_t}} - 1\right) - I_{gen} \tag{6.6}$$

$$V_t = \frac{kT}{q} \tag{6.7}$$

where I_s is the saturation current, V_t the thermal voltage described by Boltzmanns constant, temperature, and the electron charge. I_{gen} is the current generated by the incident photons and n is the ideality factor. For Si-based diodes this factor takes a value between 1 and 2 indicating a diode current governed by diffusion or space charge recombination respectively.

As described in section 3.2.3 the concentration levels of the p-type and n-type regions are of the same magnitude. This results in a situation where the injected minority carrier concentration is comparable to the majority carrier concentration – called high level injection. In this domain the space charge recombination is dominant, hence a n factor of 2 is expected [18]. The saturation current can be calculated from equation (6.8), which expresses the current as a product of the the saturation current density J_{sscr} for space charge recombination and the cross sectional area A of the junction:

$$I_s = J_{sscr}A = \frac{qn_i x_d}{2\tau_p}A \tag{6.8}$$

where the depletion width x_d, carrier lifetime τ_p and the build-in voltages V_{bi} are given by:

$$x_d = \sqrt{\frac{2\epsilon}{q}\left(\frac{N_a + N_d}{N_a N_d}\right) V_{bi}} \tag{6.9}$$

$$\tau_p = {L_n}^2 / D_n \tag{6.10}$$

$$V_{bi} = V_t \ln\left(\frac{N_a N_d}{{n_i}^2}\right) \tag{6.11}$$

yielding:

$$I_s = \frac{n_i D_n A}{2{L_n}^2}\sqrt{2\epsilon kT\left(\frac{N_a + N_d}{N_a N_d}\right)\ln\left(\frac{N_a N_d}{{n_i}^2}\right)} \tag{6.12}$$

The diode voltage V_d for a non ideal diode can be expressed as the measured voltage V_a minus the voltage drop due to series resistance R_s. Combined with equation (6.6) this yields:

$$V_a = R_s I_d + n V_t \ln\left(\frac{I_d + I_s}{I_s}\right) \tag{6.13}$$

Equation (6.13) will later be used to determine the diode performance parameters from experimental data sets.

Obtaining the data needed for the IV characteristic requires a probe station and e.g. a HP 4145B Semiconductor Parameter Analyser. The probe station is a measuring device made at MIC for general electrical testing of devices. It is equipped with a number of probes which can be translated in all three directions and are connected to external equipment through low-noise cables. The station is electrically screened, also with respect to ambient light if so desired.

Each of the six diodes on the chip were in turn connected by applying the probes to the wire bonding pads. A voltage sweep from -2V to 2V with steps of 10mV and a compliance of 100mA were performed with the analyser. Figure 6.7 shows the IV characteristic for a reference cell where the photo current I_{gen} – difference in the dark/light reverse current – can be read to be approximately 10μA.

Generally MatLab has been used for numerical calculations, but in this case a nonlinear curve fit was required, which MatLab does not support unless a routine is made. Therefore the program Origin60 was used for the curve fitting. Fitting equation (6.13) to the forward biased part of figure 6.7 results in the following values:

$$R_s = 15.8\Omega \qquad I_s = 1.3 \cdot 10^{-9}\text{A} \qquad nV_t = 0.048\text{V}$$

which results in a n factor of 1.86 as expected due to the large depletion region described in section 3.2.3. These and the following values have been

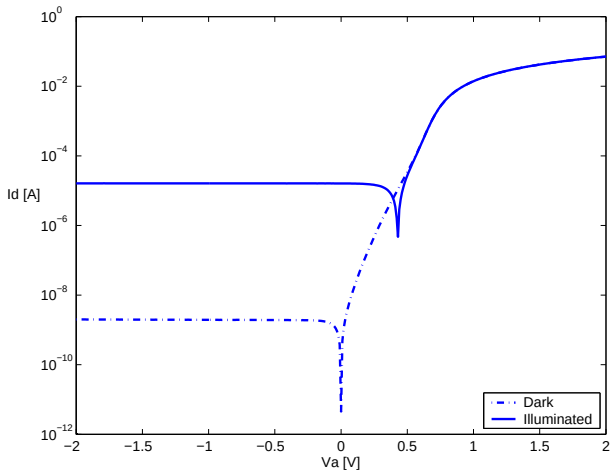


Figure 6.7: IV characteristic for the horizontal reference area on chip 21.

calculated for a temperature of 300K. Results from the horizontal areas of chip no. 21 and 71 are summarized in table 6.2 and the corresponding graphs can be found in appendix D. Generally the measured diodes exhibits poor n values and in one case high saturation current. Inserting the impurity concentrations given in section 3.2.3 in equation (6.12) and assuming a diffusion length L_n of 10μ gives an estimate for the space charge recombination dominated saturation current of 567nA and 662nA for a reference and a triangular area respectively ($L_n = 100\mu$m gives 5.67nA and 6.62nA). The cross sectional area used for this estimate is calculated as the circumference of the sensor area in question times the thickness of the device layer. It should be noted that I_s is dependant on the diffusion length squared, suggesting the value of L_n varies for each diode. The difference in measured values and the ideal is ascribed recombination due to traps in both the buried oxide and the oxide constituting the antireflective layer [15]. A series of optical test were conducted following the dicing of the wafer. The best performing chips were used for DTUsat, therefore the chips used for this electrical characterisation are of a lower quality.

Diode id	$R_s[\Omega]$	I_s [nA]	nV_t [V]	n
21Href	15.8	1.3	0.048	1.86
21Hcon	25.5	21.8	0.072	2.79
21Hmid	59.7	9.0	0.064	2.48
71Href	19.1	10.7	0.055	2.13
71Hcon	30.0	69.4	0.081	3.13
71Hmid	37.2	237.1	0.091	3.52

Table 6.2: Diode parameters.

6.4 Calibration of Flight Sensors

Requirements from the payload to attitude determination are quite low; the accuracy obtained by investigating the mechanical assembly is simply enough. Therefore no calibration was performed to establish relations between sensors and the body frame.

However, to enable in space validation of DTUsat's sun sensors and magnetometer [23] precise co-calibration is desired. This calibration was accomplished with a variety of the method proposed by Merayo *et. al* [28]. By doing half-sphere measurements on a known constant magnetic field and a known solar position with the magnetometer and each sun sensor respectively the desired sun sensor-magnetometer relations can be determined to great accuracy. The measurements were performed before launch, but the data will not be treated in this report since it is beyond the scope of this project.

In addition to this calibration procedure each flight sensor was measured at many evenly distributed points over a half-sphere; cf. figure 6.8. These data should be used by the ACDS group for calibration of the measurements – evaluation of sensor outputs has been initiated in [10].

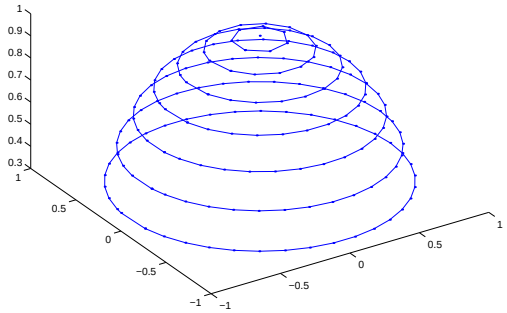


Figure 6.8: Example of measuring points for calibration of sun sensors.

7

Conclusion

A two-axis MOEMS slit sun sensor based on a well-known principle, where the generated currents in triangular sensor areas are used to calculate the angle of incidence, have been fabricated and launched into space on its first voyage on DTUsat. However, as explained in section 1.1.4 the DTUsat mission only had a limited success, which means that flight data is not available.

Compared to traditional designs the new MOEMS design has many advantages. The most obvious are that the system becomes smaller, lighter and consumes less power, which is naturally always appreciated in spacecrafts. DTUsat was among the very first CubeSats to be launched, where this specific satellite class sets severe requirements on miniaturisation since all available systems were to large to be used on such a pico satellite. The microtechnological advantages compared to traditional instrument technology also has the advantage that 100 identically mounted chips can be produced on one wafer, whereas traditional methods only produce one sensor at the time.

Furthermore this novel design has the advantage that smarter measuring principles can be utilised. In addition to the triangular sensor areas the sensor chip has reference cells, which can be used to make the device independent of various undesired parameters as described in chapter 2. The small dimensions and the use of the reference cells also makes it possible to get a linear sensor. The signal from the reference cells can also be used for on-chip temperature measurements.

This report describes the work conducted through the design, development, fabrication, testing, and integration of the sun sensor system. The MOEMS chip has a size of $\sim 7 \times 8\text{mm}^2$ and a Field of View of $\pm 70^\circ$. Preliminary laboratory measurements showed errors below 0.17° in -50° to 50°, and interpretations of this and other measurements indicates that a resolution better than 1° is obtainable for -40° to 40°. Beyond these angles a resolution below 1° is more difficult to obtain. The device is not completely

linear, but as the test results show the result is pretty good for a first generation MOEMS sensor developed in just one and a half years from the idea was conceived to launch on a satellite.

The process design of the sensor furthermore reduces the albedo dependence, which is often a problem on analog sensors. This is done in two ways. First the measuring principle with the reference areas make the sensor independent of the intensity contribution. Secondly the angular error from albedo is minimised by making the sensor more sensitive in the UV region. See sections 2.1.1, 3.2.3-3.2.4, and 6.2 for details.

Our sensor is among the very first MEMS sun sensors to be developed. NASA has developed an APS based sensor with an accuracy of 1 arcminute and a mass of 9g for use on miniature spacecrafts and planetary robotic vehicles. The developed sensor has a mass of 7.1g, and estimates have shown that it is possible to reduce the mass to approximately 3g. However, with regards to accuracy the used analog design cannot compete with the NASA APS sensor. The NASA sensor is naturally also more complete in respect to space qualification and modular encapsulation, but creating a sensor that has specifications this close to a NASA sensor is quite amazing considering the amount of time and money that was spend on the project – and considering that the project has been carried out by students in their spare time. Consult chapters 2 and 5 for more details.

The work carried out in this project has been presented at various conferences and workshops (cf. section 1.2), and this has saved the project from a desk drawer destiny. At the time of writing environmental testing has been initiated at the University of Applied Sciences Aachen, Germany, and at ESA/ESTEC, Noordwijk, the Netherlands, integration of our sensors is being conducted on SSETI Express. Hopefully the work will also be continued on future DTUsat missions, and maybe it will ultimately become a very space proven sensor that fly on many student satellites around the world.

At last the authors would like to encourage any reader with interest in the developed sensor to contact us via the following addresses, that will also remain valid when we graduate from DTU:

Martin Pedersen: http://www.skinny.dk

Jan H. Hales: http://www.hales.dk

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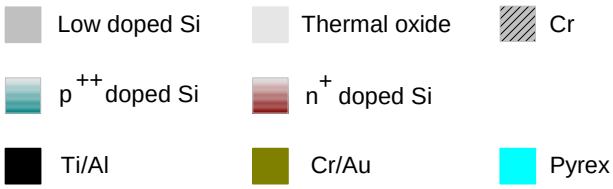
A

Process Sequence

Legend



SOI Wafer

1. RCA Cleaning

- $SC1$ for 10min.
- 5% HF for 30sec.
- $SC2$ for 10min.
- 5% HF for 30sec.

2. Oxide Growth

- 1000Å wet oxide is grown at 1000°C for 10min. in the phosphorus drive-in furnace.

3. Mask 1: p-type Wells

- HMDS furnace.
- Spinning of 1.5μm photoresist.
- UV-light exposure for 10s in the KS aligner (H-contact mode).

4. Development

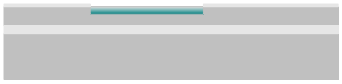
- Development in $NaOH$ for 55s.

5. Oxide Etch

- 1000Å is etched away in 5% HF (1min. and 40sec. / $600\frac{\mathring{\text{A}}}{\text{min.}}$).

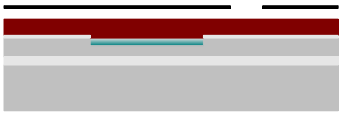
6. p-type Implantation

- BF_2 implantation with a dose of $2 \cdot 10^{11}\text{cm}^{-2}$ at 30keV.



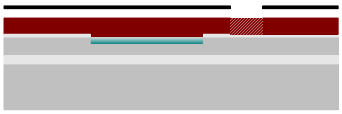
7. Resist Stripping

- Coarse stripping in acetone for 1min.
- Stripping in acetone+ultrasound for $\sim$ 5min.
- 7-UP(H_2SO_4/H_2O_2) for 10min. at 80°C



8. Mask 2+3 a): p^+-type Implantation

- HMDS furnace.
- Spinning of 1.5μm photoresist.
- UV-light exposure with mask 2 (n wells) for 10s in the KS aligner (H-contact mode).



9. Reversal Bake

- 2min. at 120°C on heating plate.

10. Mask 2+3 b): p^+-type Implantation (Flood Exposure)

- UV-light exposure with mask 3 (Contact Holes) for 25s in the KS aligner (H-contact mode).

11. Development

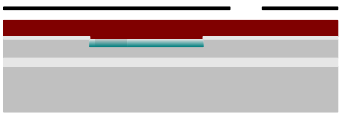
- Development in $NaOH$ for 55s.

12. p^+-type Implantation

- BF_2 implantation with a dose of $5 \cdot 10^{15}\text{cm}^{-2}$ at 30keV.

13. Resist Stripping

- Coarse stripping in acetone for 1min.
- Stripping in acetone+ultrasound for $\sim$ 5min.
- 7-UP for 10min. at 80°C



14. Mask 2: n-type Implantation

- HMDS furnace.
- Spinning of 1.5μm photoresist.
- UV-light exposure for 10s in the KS aligner (H-contact mode).

15. Development

- Development in $NaOH$ for 55s.

16. Oxide Etch

- 1000Å is etched away in 5% HF (1min. and 40sec).

17. n-type Implantation

- Phosphorous ion implantation with a dose of $5 \cdot 10^{15}\text{cm}^{-2}$ at 150keV.

18. Resist Stripping

- Coarse stripping in acetone for 1min.
- Stripping in acetone+ultrasound for $\sim$ 10min.

19. RCA and Growth of Anti-Reflective Coating

- $SC1$ for 10min.
- 5% HF for 30sec.
- $SC2$ for 10min.
- 1000Å thermal oxide(dry) is grown at 1000°C for 3hrs. in the phosphorus drive-in furnace.

20. Mask 3: Contact Holes

- HMDS furnace.
- Spinning of 1.5μm photoresist.
- UV-light exposure for 10s in the KS aligner (H-contact mode).

21. Development

- Development in $NaOH$ for 55s.

22. Etch of Contact Holes

- 1000Å is etched away in 5% HF (1min. and 40sec.).

23. Resist Stripping

- Coarse stripping in acetone for 1min.
- Stripping in acetone+ultrasound for $\sim$ 5min.
- 7-UP for 10min. at 80°C

24. Mask 4: Conducting Paths

- HMDS furnace.
- Spinning of 1.5μm photoresist.
- UV-light exposure for 10s in the KS aligner (H-contact mode).

25. Development

- Development in $NaOH$ for 55s.

26. Metal Deposition

- 150Å Ti, 2000Å Al using the Alcatel.

27. Lift Off

- Acetone+ultrasound for $\sim$ 10min.

28. Mask 5: Groove Etch

- HMDS furnace.
- Spinning of 2.6μm photoresist.
- UV-light exposure for 13s in the KS aligner (H-contact mode).
- Burning of resist

29. Development

- Development in $NaOH$ for 70s.

30. Groove Etch

- 1000Å oxide is etched away in 5% HF (1min. and 40sec).
- 2.6μm Si is etched away with RIE 18min. 30sec using the OH_POLYA recipe.
- 1μm oxide is etched away in 5% HF (14min.)

31. Resist Stripping

- RIE 3min. using the PR_STRIP recipe.

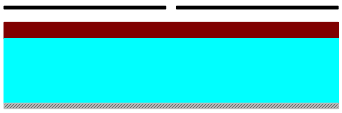
Pyrex Wafer

32. Pyrex Wafer

- Mechanical cleaning with soap and water.
- 7UP rinse for 10min.

33. Metal Deposition

- 1000Å Cr deposited using the Alcatel.



34. Mask 6:

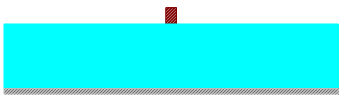
- HMDS furnace
- Spinning of 1.5μm resist.
- UV-light exposure for 4s in the KS aligner (hard contact mode).

35. Reversal Bake

- 2min at 120°C (contact heat).

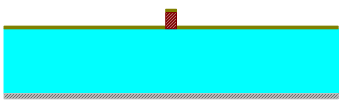
36. Flood Exposure

- 25s in the KS aligner



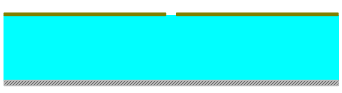
37. Development

- Development in $NaOH$ for 55s.



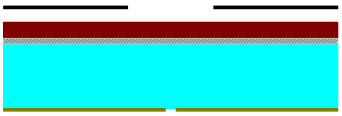
38. Metal Deposition

- 150Å Cr, 2000Å Au using the Alcatel.



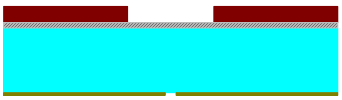
39. Liff off

- Acetone+ultrasound for $\sim$ 10min.



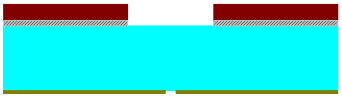
40. Mask 7

- HMDS furnace
- Spinning of 6.2μm resist(track 2).
- UV-light exposure for 55s in the KS aligner (hard-contact mode).



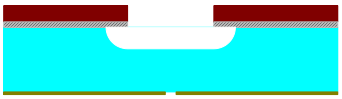
41. Development

- Development in $NaOH$ for 3min 20sec.
- Hardbake for 20min at 120°C



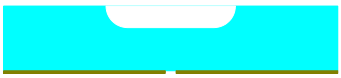
42. Cr Etch

- Blue tape on slit side.
- Wafer soaked in DI-water.
- Cr etch for approximately 10min.



43. Pyrex Etch

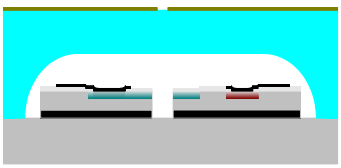
- 40%HF etch for 3min 20s (11μm).



44. Resist stripping and Cr Etch

- Removal of blue tape.
- Coarse stripping in acetone for 1min.
- Stripping in acetone+ultrasounde for 3min.
- 7UP rinse for 10min.
- Blue tape on slit side.
- Wafer soaked in DI-water.
- Cr etch till all the Cr is gone.
- Additional 7-UP if necessary.

Wafer Assembling



45. Bonding

- Anodic bonding, 700V at 350°C using a Si wafer with 160Å oxide as protection wafer.

B

Mask Documentation

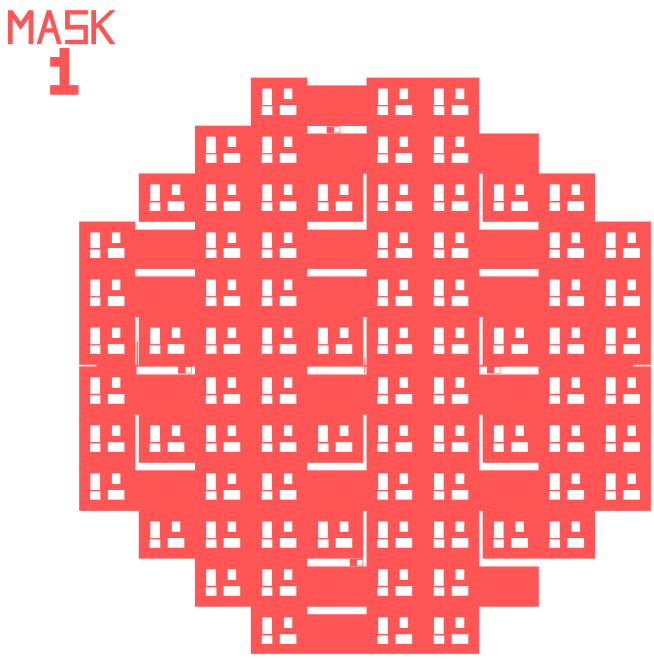


Figure B.1: Mask 1, p-type implant.

(a) (b) (c)

Figure B.2: The tree different sensors: *(a)* analog sensor, *(b)* analog sensor with fingers and *(c)* digital sensor.

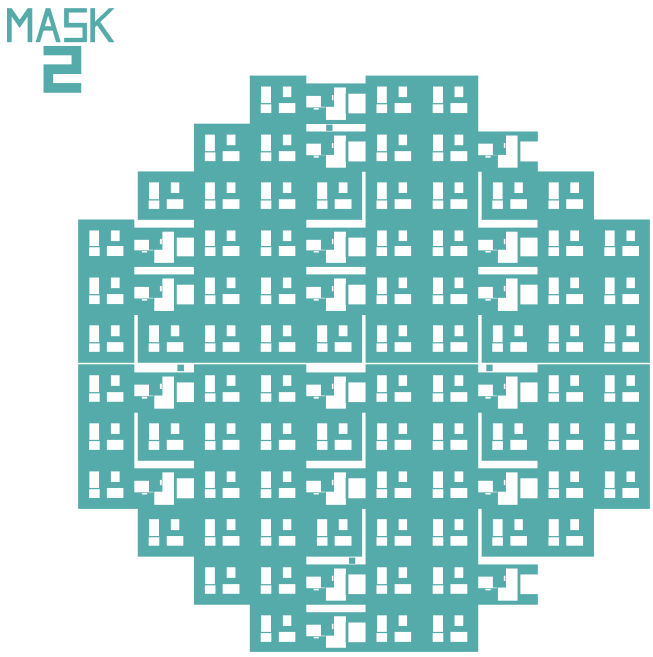


Figure B.3: Mask 2, n-type implant.

(a) (b) (c)

Figure B.4: The tree different sensors: *(a)* analog sensor, *(b)* analog sensor with fingers and *(c)* digital sensor.

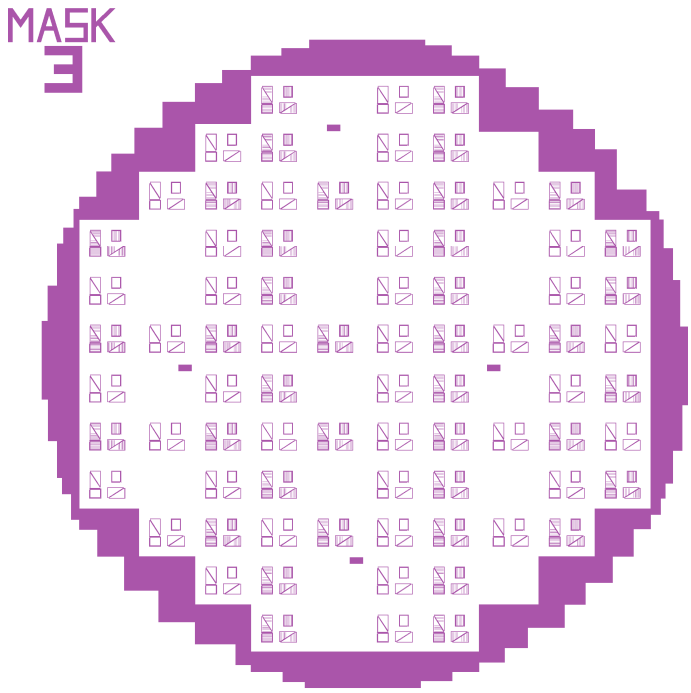
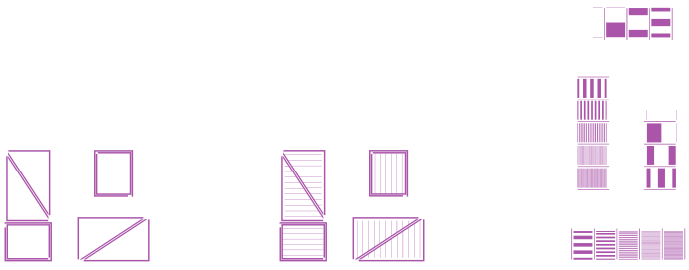


Figure B.5: Mask 3, contact holes.



(a) (b) (c)

Figure B.6: The tree different sensors: *(a)* analog sensor, *(b)* analog sensor with fingers and *(c)* digital sensor.

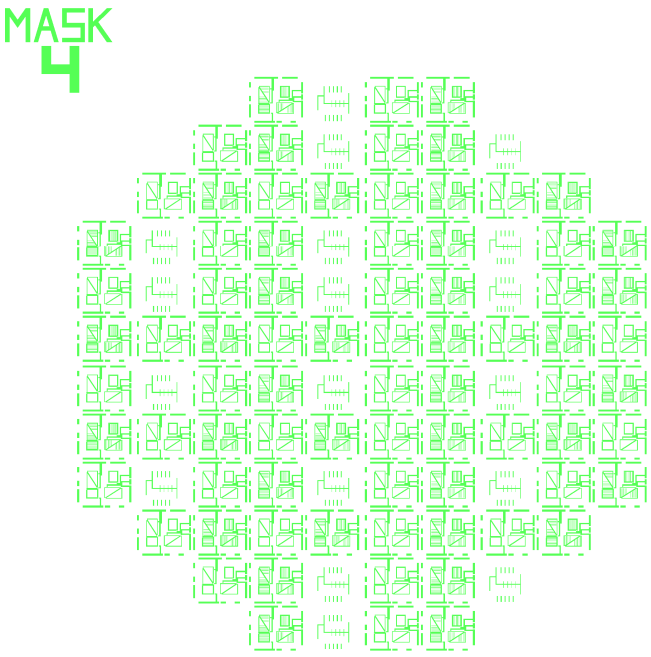
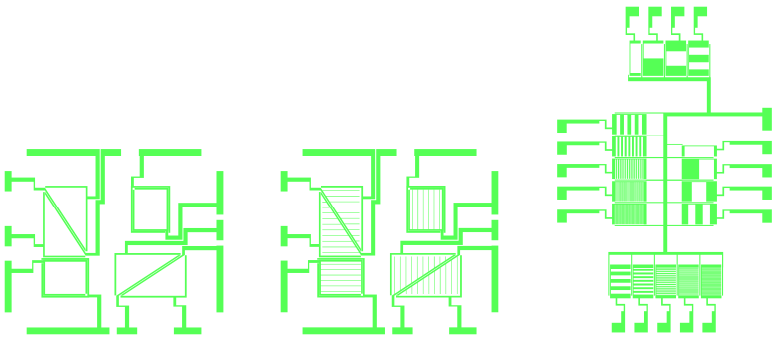


Figure B.7: Mask 4, conducting paths.



(a) (b) (c)

Figure B.8: The tree different sensors: *(a)* analog sensor, *(b)* analog sensor with fingers and *(c)* digital sensor.

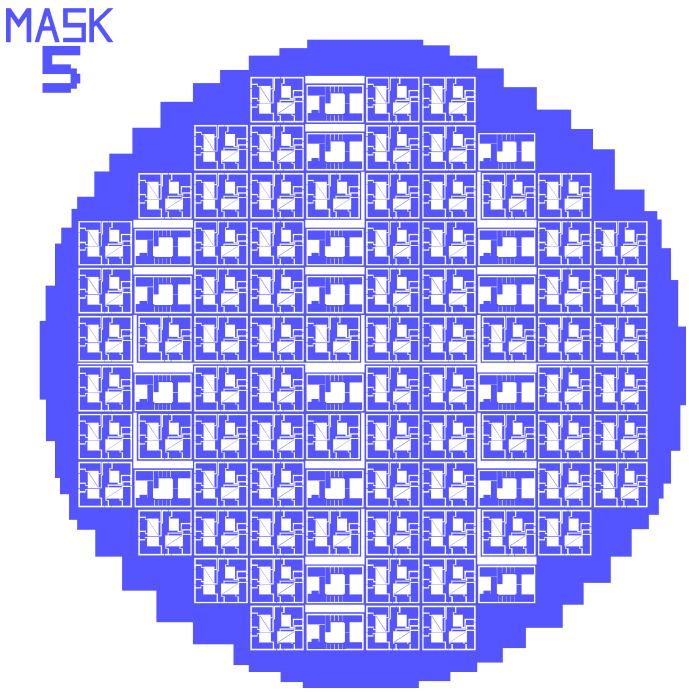
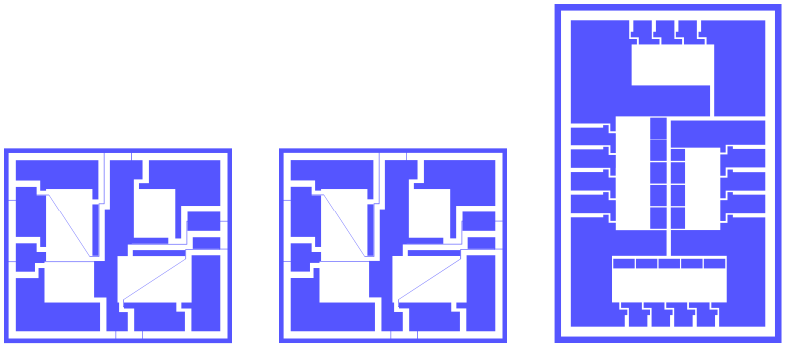


Figure B.9: Mask 5, groove etch.



(a) (b) (c)

Figure B.10: The tree different sensors: *(a)* analog sensor, *(b)* analog sensor with fingers and *(c)* digital sensor.

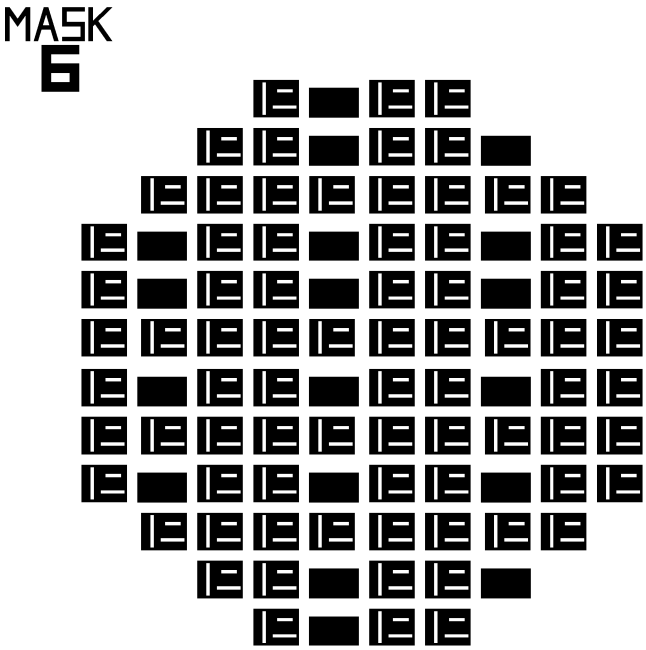
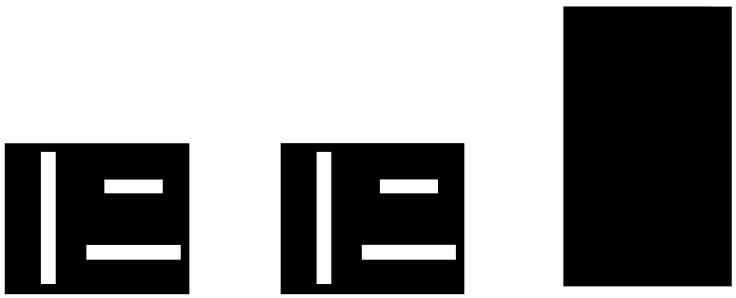


Figure B.11: Mask 6, optical slit.



(a) (b) (c)

Figure B.12: The tree different sensors: *(a)* analog sensor, *(b)* analog sensor with fingers and *(c)* digital sensor with a slit width of $1.5\mu\mathrm{m}$ (the slit is to small to be properly shown) .

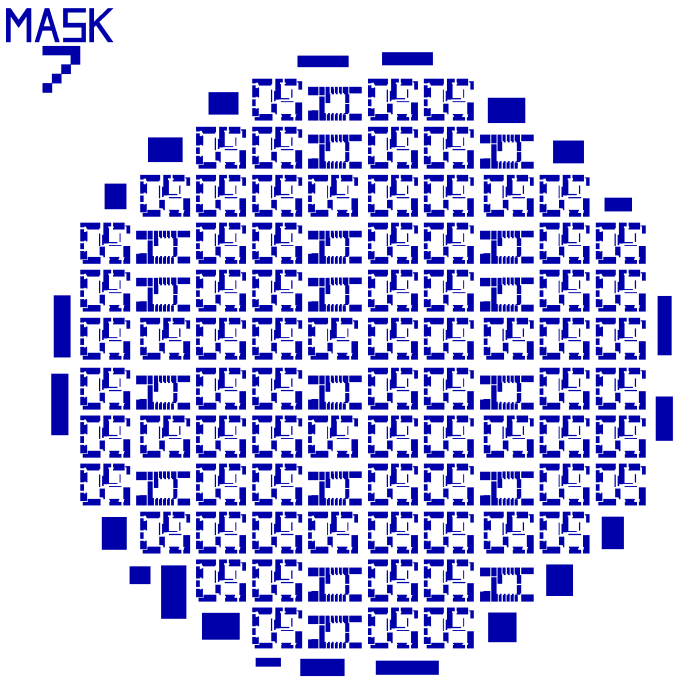
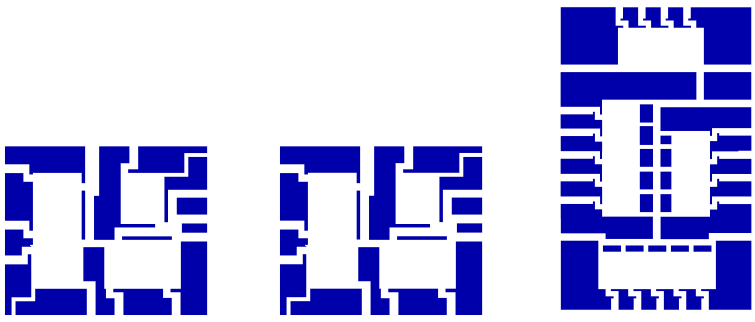


Figure B.13: Mask 7, pyrex cavity.



(a) (b) (c)

Figure B.14: The tree different sensors: *(a)* analog sensor, *(b)* analog sensor with fingers and *(c)* digital sensor.

C

Electronics Documentation

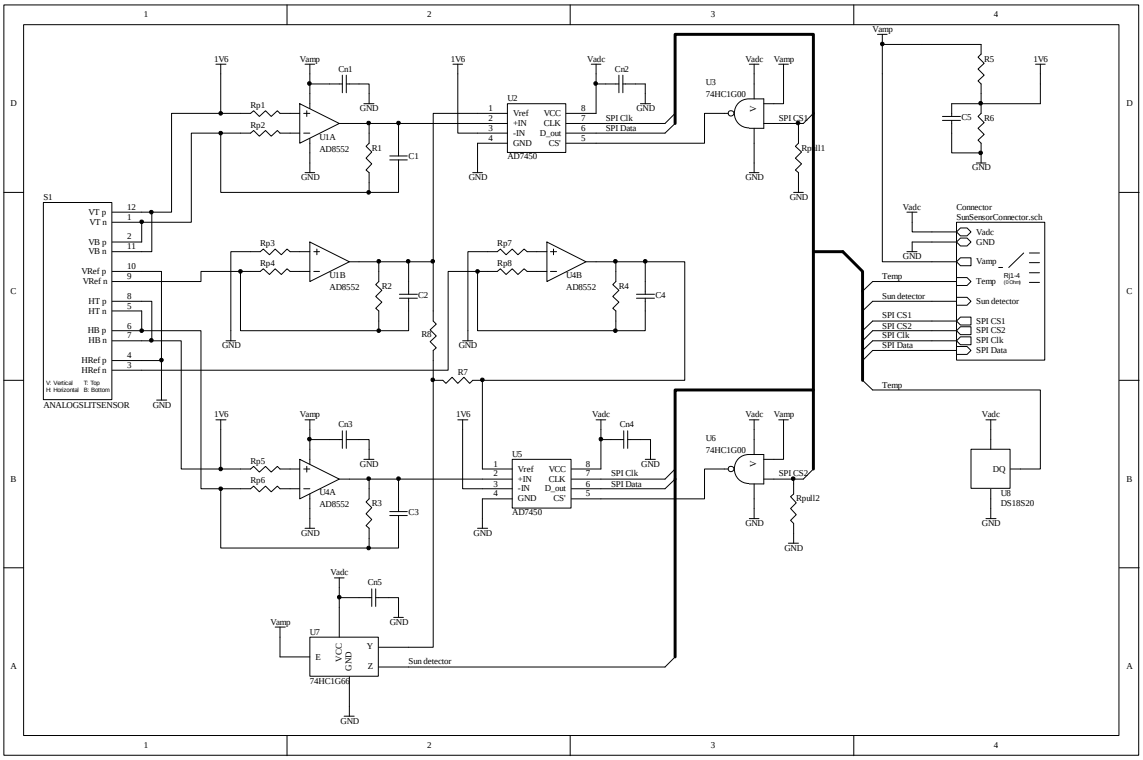


Figure C.1: Schematic of the sun sensor circuit.

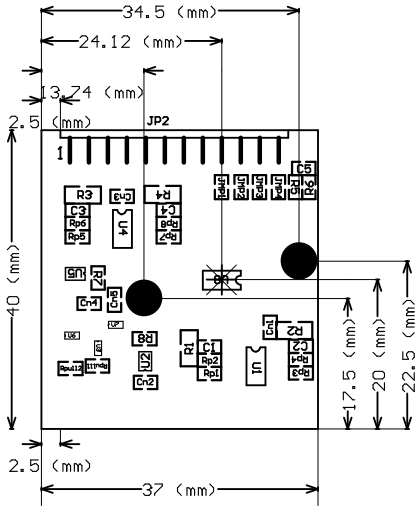


Figure C.2: Mechanical and component layout of the top layer.

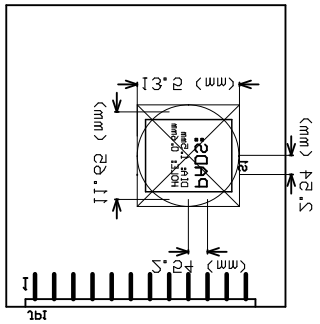
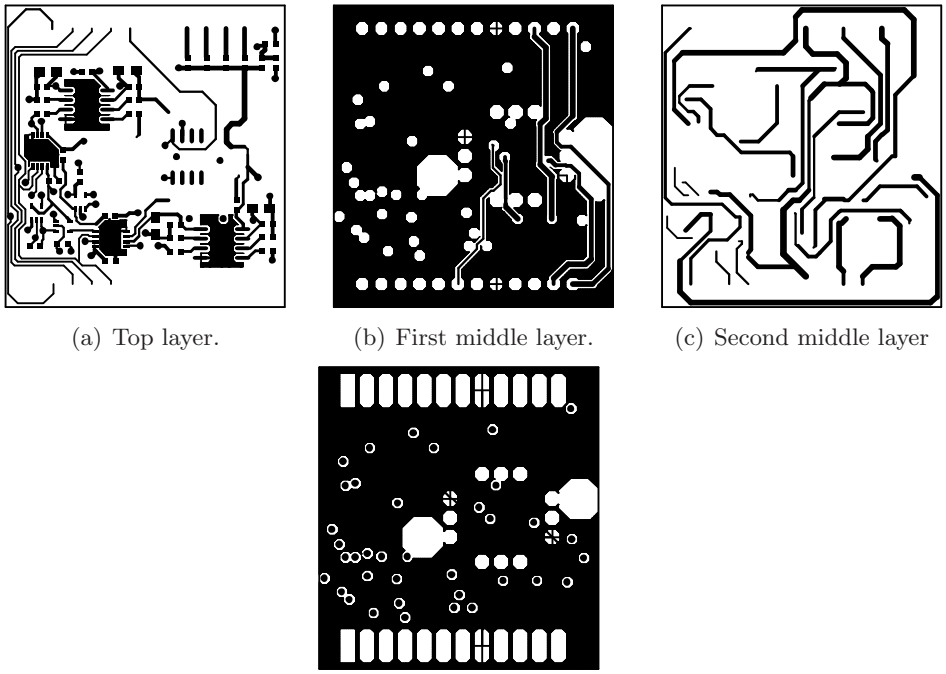


Figure C.3: Mechanical and component layout of the bottom layer.



(a) Top layer. (b) First middle layer. (c) Second middle layer

(d) Bottom layer.

Figure C.4: The four different layer constituting the PCB.

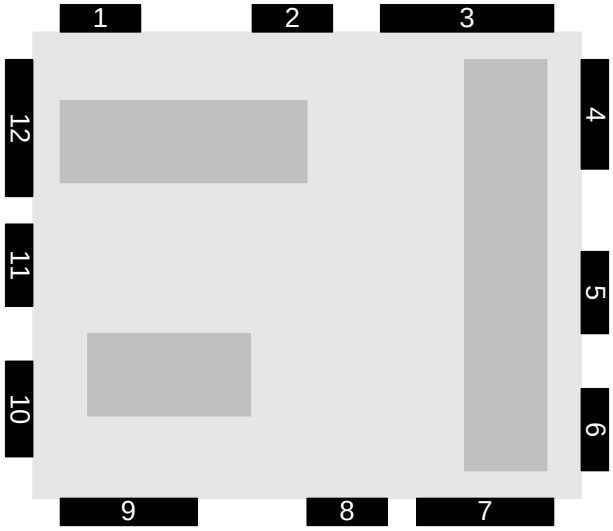


Figure C.5: Chip connections where the numbers refers to the chip areas given in table C.1.

1	2	3	4	5	6
VT n	VB p	Href n	Href p	HT n	HB p
7	8	9	10	11	12
HB n	HT p	Vref n	Vref p	VB n	VT p

Table C.1: Chip connections - see figure C.5.

Name	Size	Value
Rp1-8	0603	2k2
R1-4	0804	16k
R5-6	0603	3k9
R7-8	0603	3k3
Rpull1-2	0603	100k
JMP1-4	0603	0R0
C1-4	0603	4.7nF
C5	0603	100nF
Cn1,3	0603	0.1μF
Cn2,4,5	0603	10nF
Name	Number	Function
U1,4	AD8582	Opamp
U2,5	AD7450 BRM	ADC
U3,6	74HC1G00	Nand gate
U7	74HC1G66	Bilateral switch
U8	DS18S20	Temp sensor

Table C.2: Bill of materials. All the resistors are of 1% quality.

D

IV Characteristics

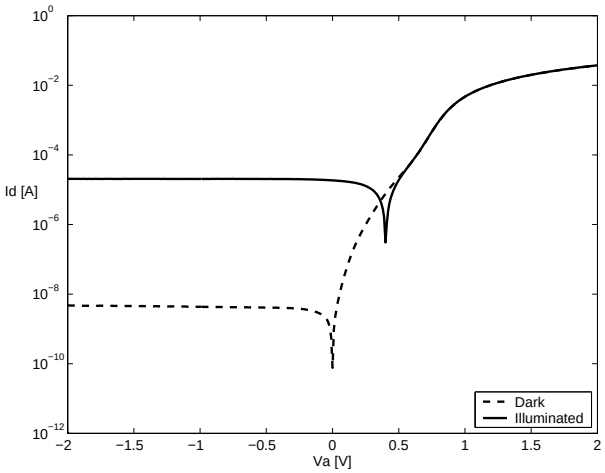


Figure D.1: First triangular area on chip 21.

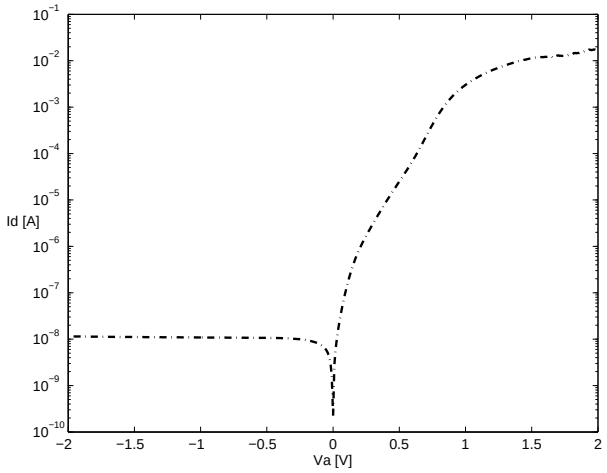


Figure D.2: Second triangular area on chip 21.

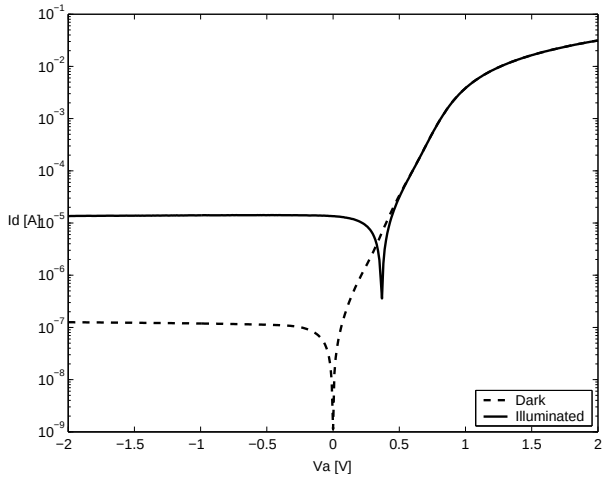


Figure D.3: First triangular area on chip 71.

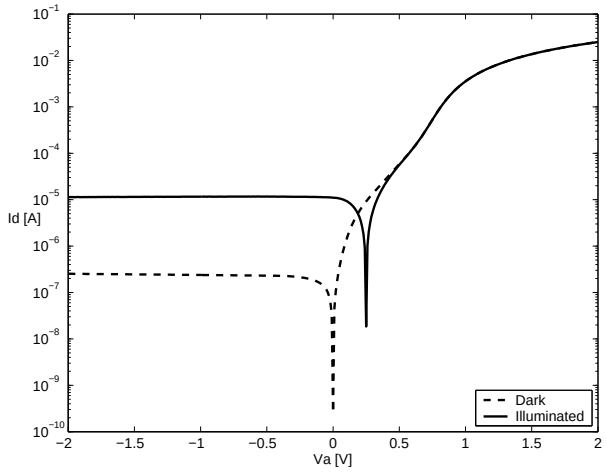


Figure D.4: Second triangular area on chip 71.

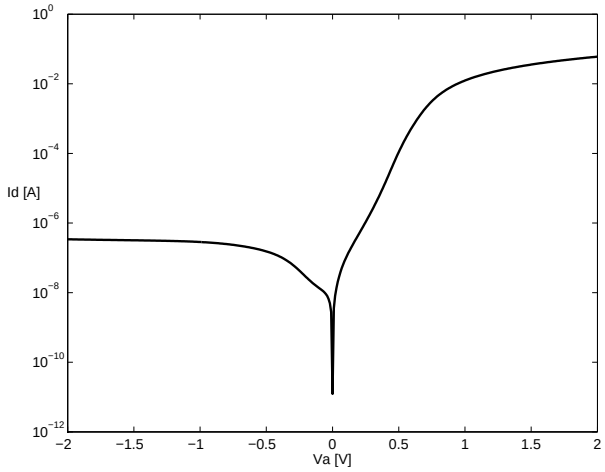


Figure D.5: Reference area on chip 71.

E

LabVIEW Programs

LabVIEW programs used for testing sun sensors before implementation on DTUsat – uses the equipment from section 6.1.1. The program for calibration of magnetometer and sun sensors is not included. A short description of the most important .vi's:

SunSensorChipAndElectroTest.vi Used for testing PCB with chip mounted. Makes a step sweep from $-70°$ to $70°$; default step size $0.1°$.

SunSensorChipAndElectroTestComprehensive.vi –,,– + it allows multiple measurements for each step. Used for e.g. checking standard deviations.

SunSensorChipAndElectroTestSphere.vi The points for measurement are equally distributed on a half sphere. A special made holder was used to realise the angles.

SunSensorChipTestNEW.vi Used for testing the chip only. Currents are generated with Keithley SourceMeters. The chip is connected to the sourcemeters with custom made connectors.

SunSensorTestComprehensive.vi Used for testing driver circuit only. Generates currents for the ideal sensor via a MatLAB script.

SPIReadSun.vi Reads sun sensor ADC.

simpleTest.vi Lets you set input currents, and outputs ADCs measurements continuously.

simpleTestSimple.vi Reads the ADCs continuously.

NOTE: When connecting the setup to a PC via the COM port we experienced problems with slow flanks. Use Schmitt triggers and the like to make nice digital output from the PC. Check it with a digital scope before starting on testing sun sensor electronics – that saves you a lot of time.

F

Monochromator

As described in section 6.2 the Jobin-Yvon H20 monochromator at MIC was automated using a DC stepping motor and a LabVIEW program. The LabVIEW program can be found on the enclosed CD-ROM.

The LabVIEW program controls the motor and measures the generated currents with Keithley Pico Ampmeters – 10 measurements for each point. Controlling the motor to precisely the same wave lengths in each run is impossible. Usually it is possible within ±2nm, but a few disagreements up to 5nm usually exist.

Jobin-Yvon H20 has an index counter display on the front, and the actual wave length of the monochromator are given as a quadratic function of this index i (the precision of this conversion is not known):

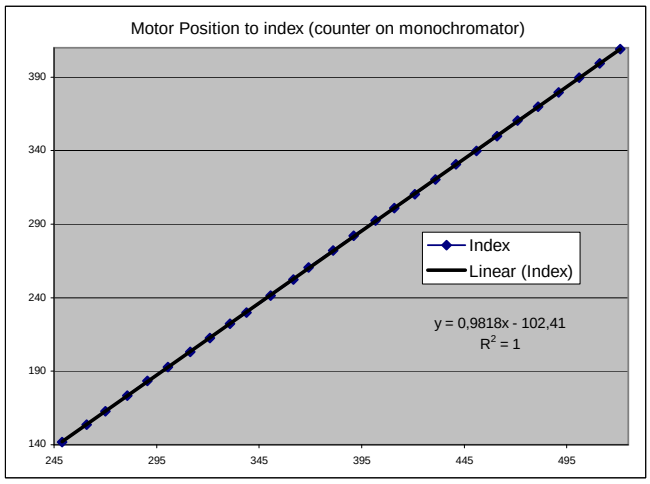
$$\lambda = -2.73 \cdot 10^{-4} i^2 + 2.2075 i - 36.688 \tag{F.1}$$

The relation between the index and the motor position was measured – and the result is found in the next section. The calibration data for the reference diode is found in the second section.

Relation between Motor Position and Index i

MotorPos	Index
248,94	141,8
261	153,6
270,13	162,8
280,65	173,3
290,55	183,3
300,61	192,9
311,36	203,3
320,96	212,5
330,77	222,2
338,8	229,9
350,58	241,4
361,66	252,4
369	260,6
380,99	272
391	282
401,66	292,5
410,94	301
420,99	310,5
431	320,5
441	330,6
450,99	339,7
461	349,9
471	360,4
481	370
490,99	379,6
501	389,7
511	399,3
521	409

Measured by: Martin Pedersen, MSc Student
MOEMS Sun Sensor
May 16, 2003



Reference Diode Calibration Data

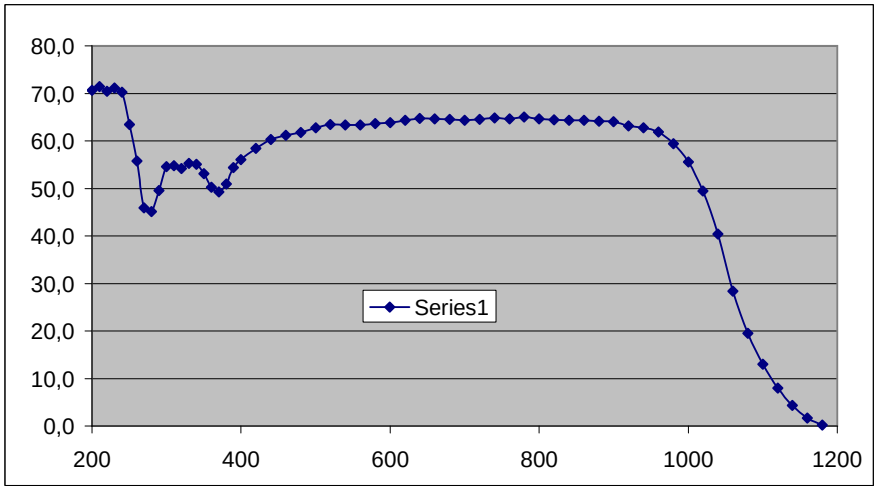
S1336-18BQ Calibration curve

S1336_18BQ calibration curve better looking 2.xls 1 W

Wavelength (nm)	Sensitivity (mA/W)	Quantum efficiency (%)	100% efficient (mA/W)	Photon energy (J)	Photon energy (eV)	Photon flux (1/s)
200	114	70,7	161	9,93E-19	6,20	1,01E+18
210	121	71,4	169	9,46E-19	5,90	1,06E+18
220	125	70,4	177	9,03E-19	5,63	1,11E+18
230	132	71,1	186	8,64E-19	5,39	1,16E+18
240	136	70,2	194	8,28E-19	5,17	1,21E+18
250	128	63,5	202	7,94E-19	4,96	1,26E+18
260	117	55,8	210	7,64E-19	4,77	1,31E+18
270	100	45,9	218	7,36E-19	4,59	1,36E+18
280	102	45,2	226	7,09E-19	4,43	1,41E+18
290	116	49,6	234	6,85E-19	4,27	1,46E+18
300	132	54,5	242	6,62E-19	4,13	1,51E+18
310	137	54,8	250	6,41E-19	4,00	1,56E+18
320	140	54,2	258	6,21E-19	3,87	1,61E+18
330	147	55,2	266	6,02E-19	3,76	1,66E+18
340	151	55,1	274	5,84E-19	3,65	1,71E+18
350	150	53,1	282	5,67E-19	3,54	1,76E+18
360	146	50,3	290	5,52E-19	3,44	1,81E+18
370	147	49,3	298	5,37E-19	3,35	1,86E+18
380	156	50,9	307	5,23E-19	3,26	1,91E+18
390	171	54,4	315	5,09E-19	3,18	1,96E+18
400	181	56,1	323	4,97E-19	3,10	2,01E+18
420	198	58,4	339	4,73E-19	2,95	2,11E+18
440	214	60,3	355	4,51E-19	2,82	2,22E+18
460	227	61,2	371	4,32E-19	2,69	2,32E+18
480	239	61,7	387	4,14E-19	2,58	2,42E+18
500	253	62,7	403	3,97E-19	2,48	2,52E+18
520	266	63,4	419	3,82E-19	2,38	2,62E+18
540	276	63,4	436	3,68E-19	2,30	2,72E+18
560	286	63,3	452	3,55E-19	2,21	2,82E+18
580	298	63,7	468	3,42E-19	2,14	2,92E+18
600	309	63,8	484	3,31E-19	2,07	3,02E+18
620	322	64,4	500	3,20E-19	2,00	3,12E+18
640	334	64,7	516	3,10E-19	1,94	3,22E+18
660	344	64,6	532	3,01E-19	1,88	3,32E+18
680	354	64,5	549	2,92E-19	1,82	3,42E+18
700	363	64,3	565	2,84E-19	1,77	3,52E+18
720	375	64,6	581	2,76E-19	1,72	3,63E+18
740	387	64,8	597	2,68E-19	1,68	3,73E+18
760	396	64,6	613	2,61E-19	1,63	3,83E+18
780	409	65,0	629	2,55E-19	1,59	3,93E+18
800	417	64,6	645	2,48E-19	1,55	4,03E+18
820	426	64,4	661	2,42E-19	1,51	4,13E+18
840	436	64,3	678	2,36E-19	1,48	4,23E+18
860	446	64,3	694	2,31E-19	1,44	4,33E+18
880	455	64,1	710	2,26E-19	1,41	4,43E+18
900	465	64,0	726	2,21E-19	1,38	4,53E+18
920	469	63,2	742	2,16E-19	1,35	4,63E+18
940	476	62,8	758	2,11E-19	1,32	4,73E+18
960	479	61,9	774	2,07E-19	1,29	4,83E+18
980	470	59,5	791	2,03E-19	1,26	4,93E+18

1000	448	55,5	807	1,99E-19	1,24	5,03E+18
1020	407	49,5	823	1,95E-19	1,22	5,14E+18
1040	339	40,4	839	1,91E-19	1,19	5,24E+18
1060	243	28,4	855	1,87E-19	1,17	5,34E+18
1080	170	19,5	871	1,84E-19	1,15	5,44E+18
1100	115	13,0	887	1,81E-19	1,13	5,54E+18
1120	72	8,0	903	1,77E-19	1,11	5,64E+18
1140	40	4,3	920	1,74E-19	1,09	5,74E+18
1160	16	1,7	936	1,71E-19	1,07	5,84E+18
1180	2	0,2	952	1,68E-19	1,05	5,94E+18

Constant of Planck, h	6,625E-34	Js
Speed of light, c	3,00E+08	m/s
Electronic charge, q	1,60E-19	C
Silicon bandgap	1,12	eV



G

Driver Specifications

These driver specifications are a work document used at the sensor implementation on DTUsat. There exist a new version which were edited by the OBC team, but we were unable to obtain it after the End of Operations of DTUsat. The document is shown here in order to give an in-sight to the interface with OBC.

The sun sensors are interfaced via the main ACDS board. To obtain knowledge of the complete ACDS driver specification the reader is encouraged also to read [22].

Registers

Control Registers

A total of 8 bytes of flash and 3 bytes of RAM are needed to hold the control information for the magnetometer as defined in table G.1.

Name	Type	SW Scope	Placement	Default
`t_warmUp`	unsigned char	Sun	Flash	? (warmup for AD8552)
`minPower`	signed char	Sun	Flash	-128d (all sides should be tested)
`illumSides`	unsigned char	Sun	RAM	00h
`shadowSIPO`	unsigned short	Sun & Mag	RAM	0000h

Table G.1: Definition of registers for sun sensor.

The number of each bit in registers and variables is designated as shown in table G.2.

...	bit 2	bit 1	bit 0
			LSB

Table G.2: Used bit notation.

t_warmup

The time it takes the system to power up.

minPower

The threshold that determines when a side receives enough sun power.

illumSides

This register is used to hold information on which sides to do measurements on. If a bit is set the corresponding side (cf. table G.3) should be measured. The order of the sides defined in `illumSides` also dictates the order in which measurements are saved in arrays (ascending order).

none	-z	-y	-x	+z	+y	+x	none
MSB							LSB

Table G.3: Definition of `illumSides`.

SIPO Shadow Register

At all times `shadowSIPO` contains the current `SIPO` setup; `SIPO` and `shadowSIPO` are defined as shown in table G.4.

`shadowSIPO` is used for making bitwise logical operations when modifying individual bits. The result is then writen to `SIPO` with MSB first, and `shadowSIPO`. `SIPO` is used by both magnetometer and sun sensors drivers, thus the common scope of `shadowSIPO`. The shadow register is placed in RAM due to the high modify rate of several times per second.

XYZSR	ZSR	YSR	XSR	XYZLS	ZLS	YLS	XLS
MSB							...

Sun2	Sun1	Sun0	XYZLP	ZLP	YLP	XLP	SensOn
...							LSB

Table G.4: Definition of `SIPO` shadow register.

Pseudo Code

The sun sensor driver consists of the functions listed in table G.5. Definitions of these in pseudo code are given in the following sections.

Function	SW Scope	Description
`SunInitialise( )`	Sun	Initialises flash registers needed by the driver.
`SunDetect( )`	Sun	Determines the sides on which sun vectors should be measured.
`SunAcquire( )`	Sun	Main function called by ACDS software to obtain the horizontal and vertical angles from a sensor.
`writeSIPO( )`	Sun & Mag	Write function for controlling the Serial Input Parallel Output device consisting of two MAX395 ICs.
`readADC( )`	Sun	Read function for reading data from the A/D converter – an ADS7817.
`Wait( )`	Global	Function to obtain an arbitrary delay of a specific number of ms (not described in the following).

Table G.5: List of functions used for the sun sensor driver.

The `SunInitialise( )` Function

This function initialises all needed flash registers in the sun sensor scope.

```
void SunInitialise( )
{
    flas_register1 := default1;
    flas_register2 := default2;
    ...
}
```

The `SunDetect( )` Function

The driver for the magnetometer contains the function `MagAcquire( )` which is the function used to obtain the current magnetic field vector in satellite body coordinates. The operation of this function is depicted in figure G.1; the figure is from [22] where additional information can be found.

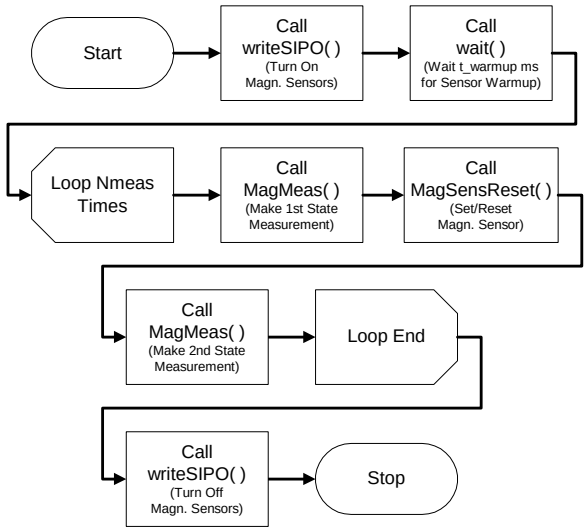


Figure G.1: Flow diagram of `MagAcquire( )`.

`MagAcquire( )`'s call to `Wait( )` should be replaced with a call to `SunDetect( )` followed by the call `Wait( t_warmup-timeof(SunDetect( )) )`.

`SunDetect( )` determines which of the satellites sides' receive enough sun power to obtain a sun vector. Pseudo code for `SunDetect( )` is given below. The function does not return anything, but saves the result in the register `illumSides`.

```
void SunDetect( )
{
    illumSides := 0;                          %Reset register

    for byte i = 1:5                          %Check the 5 sides
    {
                                              %Select side i
        writeSIPO( (shadowSIPO AND (FF1Fh+32d*i)) OR 32d*i);

        wait(t_warmUp);                       %Powering OP AMPS

                                              %More sun power than req.?
        if (readADC(SPI_SEL_(OBC-ACDS con. pin 15)) > minPower)
```

```
            illumSides(i) := 1;             %Set side i to be measured
    }

    writeSIPO( shadowSIPO AND FF1Fh );      %Deselect selected side
}
```

The `SunAcquire( )` Function

When execution of `MagAcquire( )` (cf. figure G.1) has been completed `SunAcquire( )` is executed before the magnetotorquers is turned on again. `SunAcquire( )` measures the `N` sides that receives enough sun power (found with `SunDetect( )`).

`SunAcquire( )` returns a `N`×2 array of signed shorts containing the results of the performed measurements – each side yields two measurements. The order of the measurements corresponds to the order set in `illumSides`. Pseudo code for `SunAcquire( )` is given below.

```
signed short[N] SunAcquire( )
{
    unsigned char N := 00h;                 %No. illuminated sides

                                            %Find no. illuminated sides
    for byte i = 1:6                        %Check all 6 possible sides
    {
        if (illumSides(i)==1)
            N++;
    }

    signed short measurement[N][2] := 0;      %Reset state measurements

    byte j := 0;
    for byte i = 1:6
    {
        if (illumSides(i)==1)
        {
                                            %Select side i
            writeSIPO( (shadowSIPO AND (FF1Fh+32d*i)) OR 32d*i);

            wait(t_warmUp);                 %Powering OP AMPS

                                            %Save measurements
            measurement[j][0] := readADC(SPI_SEL_(OBC-ACDS con. pin 15));
            measurement[j][1] := readADC(SPI_SEL_(OBC-ACDS con. pin 16));
            j++;
        }
    }

    writeSIPO( shadowSIPO AND FF1Fh );     %Deselect selected side

    return measurement;
}
```

The code could be optimised if smarter data types are available since the first loop determining the number of illuminated sides then could be omitted. Instead the array should simply be increased with an appropriate `arrayname.add()` function.

Note that if the implementation is to be carried out in ANSI C the mentioned loop should be moved to illumSides, and the result `N` should then be a flash register.

`writeSIPO( )` Function

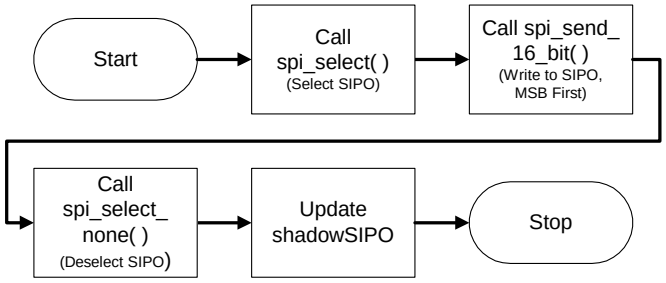


Figure G.2: Flow diagram of `writeSIPO( )`

`writeSIPO` is shared with the magnetometer driver. It is used to update `shadowSIPO`. Pseudo code for `writeSIPO( )`:

```
writeSIPO(short Value)
{
    spi_select(SPI_SEL_(OBC-ACDS con. pin 15)); %select SIPO
    spi_send_16_bit(Value);              %send value, MSB first
    spi_select_none();                   %strobe SIPO
    shadowSIPO := Value;                 %update shadowSIPO
}
```

`readADC( )` Function

Note that this function has the same name as a function in the magnetometer driver scope, and that they are not identical!

```
signed short readADC(unsigned char SPI_SEL_PIN)
{
    unsigned short res;

    spi_select(SPI_SEL_PIN);                %Select ADC

    res := spi_get_16_bit();                %Read ADC output

    %Convert to 12bit signed to signed short (16bit)
    % two's complement - it is assumed that shl shift in 0s
    res := res shl 4;

    spi_select_none();                      %Deselect ADC

    return res;
}
```

H

SOI Wafer Data Sheets

First Batch SOI wafer Specifications

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ANALOG DEVICES **Product Specification: 100.083901** **Issue Date: 23-Mar-2001**

Part Number :	**MIC005**	Date:	**15 Jan 2002**
Customer:	**Mikroelektronik Centret (DTU)**	STD:	**Y**
Customer Specification/ Reference:	**Rene Fleron**		

Category	*Parameter*	*Specification*	*Measurement Method*
Overall			
Wafer			
1.1	Diameter	100mm +/- 0.5	Wafer Vendor
1.2	Primary Flat Orientation	{110}+/- 1°	Wafer Vendor
1.3	Primary Flat Length	32.5mm +/- 2.5	Wafer Vendor
1.4	Secondary Flat Orientation	None	
1.5	Thickness	456 µm +/- 25	ADE 100%
1.6	Total Thickness Variation(TTV)	< 5µm	Guaranteed by Process
1.7	Bow	< 60µm	ADE to ASTM F534, 20%
1.8	Warp	< 60 µm	ADE to ASTM F657, 20%
1.9	Edge Chips	0	Bright Light, 100%[1]
1.10	Edge Exclusion	5mm	
Handle			
Silicon			
2.1	Growth Method	FZ	Wafer Vendor
2.2	Orientation	{100}+/- 1°	Wafer Vendor
2.3	Thickness	450µm +/- 5µm	ADE, 100%
2.4	Doping type	N	Wafer Vendor
2.5	Dopant	Phosphorous	Wafer Vendor
2.6	Resistivity	3-5 ohm-cm	Wafer Vendor
2.7	Backside Finish	Lapped/etched	Wafer Vendor
Buried			
Oxide			
3.1	Oxide Type	Thermal	
3.2	Oxide Thickness	1000nm +/- 50nm	Nanospec centre point, 4%
3.3	Oxide formed on	Handle Wafer	

Category	*Parameter*	*Specification*	*Measurement Method*
Device			
Silicon			
4.1	Growth Method	CZ	Wafer Vendor
4.2	Oxygen Concentration	<8E17 cm^{-3}	Wafer Vendor
4.3	Carbon Concentration	<2E15 cm^{-3}	Wafer Vendor
4.4	Orientation	{100}+/- 1^{o}	Wafer Vendor
4.5	Nominal Thickness	5µm	FTIR / ADE, 100%
4.6	Thickness Variation	+/-0.5µm	FTIR/ ADE, 100% 5-Pt[2]
4.7	Distance to device silicon		
	edge from wafer edge	<5mm	Typical by process
4.8	Doping Type	N	Wafer Vendor
4.9	Dopant	Phosphorous	Wafer Vendor
4.10	Resistivity	20-40 ohm-cm	Wafer Vendor
4.13	Voids	0	Bright Light, 100%[1]
4.14	Scratches	<25mm total length	Bright Light, 100%[1]
4.15	Haze	None	Bright Light, 100%[1]

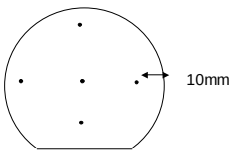
Shipping Details

Wafers per box	25 maximum
Packaging	Taped Polypropylene Wafer Box Empak, Ultrapak, 100mm Antistatic Double Bagging
Lot Shipment Data :	Device Silicon Thickness

Explanatory Notes

1. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in 1.11. High intensity bright lamp inspection as per ASTM F523.

2. 5 point measurement is centre and 4 points 10mm from edge of wafer.



Approvals	Quality:	Engineering:	Marketing:

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New Batch - SOI Wafers with 500nm BOX

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ANALOG DEVICES **Product Specification:100.111601** **Issue Date: 30-May-2002**

Part Number :	**MIC006**	Date:	**18-December-2002**
Customer:	**MIC**	STD:	**Y**
Customer Specification/ Reference:	**Rene Fleron**		

Category	*Parameter*	*Specification*	*Measurement Method*
Overall			
Wafer			
1.1	Diameter	100 +/- 0.5 mm	Wafer Vendor
1.2	Primary Flat Orientation	{110}+/- 1°	Wafer Vendor
1.3	Primary Flat Length	32.5 +/- 2.5 mm	Wafer Vendor
1.4	Secondary Flat Orientation	None	
1.5	Thickness	406 +/- 7 µm	ADE, 100%
1.6	Total Thickness Variation(TTV)	< 5µm	Guaranteed by Process
1.7	Bow	< 100 µm	ADE to ASTM F534, 20%
1.9	Warp	< 100 µm	ADE to ASTM F657, 20%
1.9	Edge Chips	0	Bright Light, 100%[1]
1.10	Defect Exclusion Radius	5mm	
Handle			
Silicon			
2.1	Growth Method	FZ	Wafer Vendor
2.2	Orientation	{100}+/- 1°	Wafer Vendor
2.3	Thickness	400 µm +/- 5µm	ADE, 100%
2.4	Doping type	P	Wafer Vendor
2.5	Dopant	Boron	Wafer Vendor
2.6	Resistivity	1-10 Ω-cm	Wafer Vendor
2.7	Backside Finish	Polished	Wafer Vendor
Buried			
Oxide			
3.1	Oxide Type	Thermal	
3.2	Oxide Thickness	500 nm +/- 25nm	Nanospec centre point, 4%
3.3	Oxide formed on	Device Wafer	

Category	Parameter	Specification	Measurement Method
Device			
Silicon			
4.1	Growth Method	FZ	Wafer Vendor
4.2	Orientation	{100}+/- 1°	Wafer Vendor
4.3	Nominal Thickness	5.5 µm	FTIR, 100%
4.4	Thickness Variation	+/- 0.5 µm	FTIR, 100% 5-Pt[2]
4.5	Distance to device silicon		
	edge from wafer edge	<5mm	Guaranteed by process
4.6	Doping Type	N	Wafer Vendor
4.7	Dopant	Phosphorous	Wafer Vendor
4.8	Resistivity	1-10 Ω-cm	Wafer Vendor
4.9	Device Side Scribe	N/A	
4.10	Voids	0	Bright Light, 100%[1]
4.11	Scratches	<25mm total length	Bright Light, 100%[1]
4.12	Haze	None	Bright Light, 100%[1]

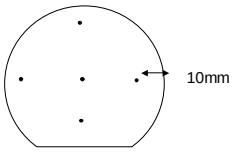
Shipping Details

Wafers per box	MAX 25
Packaging	Taped Polypropylene Wafer Box Empak, Ultrapak, 100mm Antistatic Double Bagging
Lot Shipment Data :	Device Silicon Thickness Bow/Warp Data

Explanatory Notes

1. All bright light inspections performed exclude all wafer area outside the edge exclusion defined in 1.10. High intensity bright lamp inspection as per ASTM F523.

2. 5 point measurement is centre and 4 points 10mm from edge of wafer.



Approvals	Quality:	Engineering:	Marketing:

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I

LAB LOG

Wafer	Purpose
BST1	Anodic bonding and RIE
BST2	Anodic bonding and RIE
BST3	Lithography using two masks
BST4	Lithography using two masks
BST5	Lithography using two masks
SEMI1	Optimizing the SOI process sequence and Anodic bonding(AB)
SEMI2	Optimizing the SOI process sequence
SEMI3	Optimizing the SOI process sequence and Anodic bonding
SEMI4	Optimizing the SOI process sequence and AB
SEMI5	Lifetime scan after first oxide growth and lithography using two masks
SEMI6	Lifetime scan after first oxide growth and ion implant
SEMI7	Lifetime scan after first oxide growth and ion implant
SEMI8	Lifetime scan after first oxide growth and ion implant
SEMI9	Optimizing the SOI process sequence and AB
SEMI10	Oxide etch with RIE
SEMI11	Oxide growt
SOI1	Final device fabrication
SOI2	Final device fabrication
SOI2	Final device fabrication

Wafer	Purpose
P1	Lithography with 4.2μ resist
P2	Al and poly-Si as cavity masking material
P3	Cavity etch with Al and poly-Si as masking material
P4	Cavity etch with Al and poly-Si as masking material and AB
P5	Cavity etch with Al and poly-Si as masking material and AB
P6	Cavity etch with Al and poly-Si as masking material and AB
P7	Lithography with 4.2μ resist
P8	Cavity etch with Al and poly-Si as masking material
P9	Lithography with 4.2μ resist
P10	Poly-Si and Cr deposit
P11	Cr deposit
P12	Cr deposit
P13	Poly-Si and Cr deposit
P14	Poly-Si and Cr deposit
P15	Poly-Si and Cr deposit
P16	Poly-Si and Cr deposit
P17	Poly-Si and Cr deposit
P18	Lithography with 4.2μ resist
P19	Lithography with 4.2μ resist
P20	Poly-Si deposit
PS1	Slit generation, cavity etch with Cr and AU as masking material
PS2	Slit generation, cavity etch with Cr and AU as masking material
PS3	Slit generation, cavity etch with Cr and AU as masking material
PW1	Slit generation and cavity etch with Cr as masking material
PW2	Slit generation and cavity etch with Cr as masking material
PW3	Slit generation, cavity etch with Cr as masking material and AB
PW4	Slit generation and cavity etch with Cr as masking material
PW5	Slit generation, cavity etch with Cr as masking material and AB
PW6	Slit generation
PW7	Slit generation and cavity etch with Cr as masking material
PW8	Final Pyrex processing
PW9	Final Pyrex processing
PT1	AB
PX1	KOH etch of poly-Si
PX2	KOH etch of poly-Si

	Wafer	BST1
	Process	**Parameters and comments**
0	Wafer Type	n-type <100>, ON73
1	HMDS	30 min.
2	SSI track1	PR2_2
3	Aligner(KS)	13 sec. HC: Mask no. 5.
4	Developer	70 sec.
5	RIE2	OH_polya. 10 min.
6	Tencore	6,1µm step centre. 6,2µm step side.
7	RIE2	OH_polya. 5 min.
8	Tencore	8,1µm step centre. 8,3µm step side.
9	Acetone	0/10 min.
10	Tencore	6,5µm step centre. 6,8µm step side.
11	Anodically bonded to PW3	650-700V at 350C.

	Wafer	BST2
	Process	**Parameters and comments**
0	Wafer Type	n-type <100>, ON73
1	HMDS	30 min.
2	SSI track1	PR2_2
3	Aligner(KS)	13 sec. HC: Mask no. 5.
4	Developer	70 sec.
5	RIE2	OH_polya. 10 min.
	RIE2	OH_polya. 4 min. 30 sec.
6	Acetone	0/10 min.
7	Tencore	6,2µm step centre. 6,4µm step side.
8	HMDS	30 min.
9	Acetone	0/3 min.
10	Anodically bonded to PW2	850V, 350C

	Wafer	BST3
	Process	**Parameters and comments**
0	Wafer Type	n-type <100>, ON73
1	HMDS	30 min.
2	SSI track1	PR2_2
3	Aligner(KS)	13 sec. HC: Mask no. 5.
4	Developer	70 sec.
5	RIE2	OH_polya. 14 min.
6	Acetone	0/10 min.
7	Tencore	6,0µm step centre. 6,1µm step side.
8	HMDS	30 min.
9	SSI track2	PR6_2
10	Aligner(KS)	15 sec. HC. Mask no. 1
11	Reversal Bake	2 min. 120C contact heat.
12	Aligner(KS)	40 sec. HC. Mask no. 5
13	Developer	3 min. 20 sec.
14	Optical Microscope	Not aligned.
15	Acetone	0/10 min.

	Wafer	BST4
	Process	**Parameters and comments**
0	Wafer Type	n-type <100>, ON73
1	HMDS	30 min.
2	SSI track1	PR2_2
3	Aligner(KS)	13 sec. HC: Mask no. 5
4	Developer	65 sec.
5	RIE2	OH_polya. 15 min.
6	Tencore	7,8µm step everywhere
7	Acetone	0/10 min.
8	Tencore	6,1µm step centre. 6,3µm step side.
9	HMDS	30 min.
10	SSI track2	PR6_2
11	Aligner(KS)	13 sec. HC: Mask no. 1
12	Reversal bake	2 min. 120C. Contact heat.
13	Aligner(KS)	35 sec. HC: Mask no. 5.
14	Developer	3 min. 25 sec. Seems to be a thin resist film left.
15	Alcatel	150/2000Å Cr/Au
16	Lift-off	10 min. CB-trix#4 did not work, gold on the wrong side of groove.

	Wafer	BST3
	Process	**Parameters and comments**
0	Wafer Type	n-type <100>, ON73
1	HMDS	30 min.
2	SSI track1	PR2_2
3	Aligner(KS)	13 sec. HC: Mask no. 5
4	Developer	65 sec.
5	RIE2	OH_polya. 15 min.
6	Acetone	0/10 min.
7	HMDS	30 min.
8	SSI track2	PR6_2
9	Aligner(KS)	17 sec. HC: Mask no. 1
10	Reversal bake	2 min. 120C. Contact heat.
11	Aligner(KS)	40 sec. HC: Mask no. 5
12	Developer	3 min. 25 sec. Seems to be a thin resist film left.
13	Developer	40 sec. HC: Mask no. 5. Film not gone.
14	Alcatel	150/2000Å Cr/Au
15	Lift-off	10 min. CB-trix#4 did not work, gold on the wrong side of groove.

	Wafer	SEMI 1
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	RCA2	10 min.
4	HF	15 sec.
5	Phosphor Drive	WET950, 45 min. No ox. was grown! Due to prog. failure
6	Phosphor Drive	WET1000, 12 min.
7	HMDS	30 min.
8	SSI track1	JTC4_2, relatively poor spinning of resist.
9	Aligner (EVC)	16 sec. Hard Contact mode
10	Developer	3 min 20 sec.
11	HF 5%	4 min 30 sec.
12	Implantation	WRONG IMPLANTATION, TOO HIGH DOSE
13	RIE	OH_POLYA, 2 min 30 sec. Removal of implantet layer
14	Acetone	20 min. Not sufficient
15	RIE	PR_STRIP, 10 min.
16	HMDS	30 min.
17	SSI track1	PR1_5
18	Aligner (EVC)	8 sec.
19	Developer	55 sec.
20	Acetone	3 min.
21	Acetone + sonic	21 min.
22	RIE	PR_STRIP, 10 min.
23	RCA 1	13 min. 67C
24	RCA 2	10 min. 68C
25	Phosphor Drive	DRY1000, 3 hours
26	HMDS	30 min.
27	SSI track1	PR1_5
28	Aligner (KS)	19 sec.
29	Developer	55 sec.
30	RIE	MP_SOI2
31	Acetone	1 min. / 15 min. Some resist is still left.
32	RIE	PR_STRIP, 10 min.
33	HMDS	30 min.
34	SSI track1	PR1_5
35	HMDS	30 min.
36	SSI track1	PR1_5
37	Aligner(KS)	10 sec. Wrong AM
38	Developer	55 sec.
39	Acetone	10 min.
40	HMDS	30 min.
41	SSI track1	PR1_5
42	Aligner(KS)	10 sec.
43	Developer	60 sec.
44	Alcatel	150/2000 Å Ti/Al
45	Lift off	10 min.
46	HMDS	30 min.
47	SSI track1	PR1_5
48	Aligner(KS)	10 sec. Complicated to align
49	Optical microscope	seems to be aligned O.K.
50	RIE	MP_SOI2, 3 min.
51	RIE	OH_POLYA, 10 min, 30 W
52	Tencor	2,6µ step. Should be 6,6µ step.
53	RIE	OH_POLYA, 8 min, 30 W
54	Tencor	4µ to 6µ step from center to edged of the wafer.
55	RIE	OH_POLYA, 4 min, 30 W
56	Tencor	5µm to 6µm step from center to edged of the wafer.
57	RIE	OH_POLYA, 4 min, 30 W
58	Tencor	5,6µm everywhere !?
59	Anodically bonded to P5	

	Wafer	SEMI 2
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	RCA2	10 min.
4	HF	15 sec.
5	Phosphor Drive	WET950, 45 min. No ox. was grown! Due to prog. failure
6	Phosphor Drive	WET1000, 12 min.
7	HMDS	30 min.
8	SSI track1	JTC4_2, relatively poor spinning of resist.
9	Aligner (EVC)	16 sec. Hard Contact mode
10	Developer	3 min 20 sec.
11	HF 5%	4 min 30 sec.
12	Implantation	WRONG IMPLANTATION, TOO HIGH DOSE
13	RIE	OH_POLYA, 2 min 30 sec. Removal of implantet layer
14	Acetone	20 min. Not sufficient
15	RIE	PR_STRIP, 10 min.
16	HMDS	30 min.
17	SSI track1	PR1_5
18	Aligner (EVC)	8 sec.
19	Developer	55 sec.
20	Acetone	3 min.
21	Acetone + sonic	21 min.
22	RIE	PR_STRIP, 10 min.
23	RCA 1	13 min. 67C
24	RCA 2	10 min. 68C
25	Phosphor Drive	DRY1000, 3 hours
26	HMDS	30 min.
27	SSI track1	PR1_5
28	Aligner (KS)	19 sec.
29	Developer	55 sec.
30	RIE	MP_SOI2
31	Acetone	1 min. / 15 min. Some resist is still left.
32	RIE	PR_STRIP, 10 min.
33	HMDS	30 min.
34	SSI track1	PR1_5
35	HMDS	30 min.
36	SSI track1	PR1_5
37	Aligner(KS)	10 sec. Wrong AM
38	Developer	55 sec.
39	Acetone	10 min.
40	HMDS	30 min.
41	SSI track1	PR1_5
42	Aligner(KS)	10 sec.
43	Developer	60 sec.
44	Alcatel	150/2000 Å Ti/Al
45	Lift off	10 min.
46	HMDS	30 min.
47	SSI track1	PR1_5
48	Aligner(KS)	10 sec. Complicated to align
49	Optical microscope	some misalignment
50	RIE	MP_SOI2, 5 min.
51	RIE	OH_POLYA, 10 min, 30 W
52	RIE	OH_POLYA, 10 min, 30 W
53	RIE	OH_POLYA, 10 min, 300 W
54	RIE	OH_POLYA, 10 min, 300 W, no EPD (no EPD detector)
55	Tencore	12µm step. Also a smaller step of 4µm.

	Wafer	SEMI 3
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	HF 5%	15 sec.
4	RCA2	10 min.
5	Phospher Drive	WET1000, 10 min.
6	SSI track1	PR2_2
7	Acetone	5 min. Forgot HMDS
8	HMDS	30 min.
9	SSI track1	PR2_2
10	Aligner(KS)	13 sec. Hard contact.
11	Developer	60 sec.
12	Hard bake	20 min. 250C, ovn
13	RIE	MP_SOI2, 3 min.
14	Tencor	2,7-2,4µm step in center. 2,8-2,5µm at edged
15	RIE	OH_POLYA, 10 min.
16	Tencor	4,9-4,6µm step in center. 5,02-4,8µm at edged
17	RIE	OH_POLYA, 10 min.
18	RIE	MP_SOI2, 15 min.Thin film left. Newton rings.
19	Tencor	7,2µm step in center. 6,9-7,16µm at edged
20	RIE	MP_SOI2, 3 min. Newton rings are not gone.
21	RIE	PR_STRIP, 10 min.
22	Tencor	6µm step in center. 6,2µm middle. 6µm at edged.
23	BHF	10 sec. + 20 sec. N-rings abit smaller.
24	RIE	PR_STRIP, 10 min. The rings was not polymer remains.
25	BHF	1 min. Mabye thin layer in center, but else gone.
26	RCA-1	13min
27	7-UP	5min
28	Anodically Bonded to P6	850V at 320C

	Wafer	SEMI 4
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	HF 5%	15 sec.
4	RCA2	10 min.
5	Phospher Drive	WET1000, 10 min.
6	HMDS	30 min.
7	SSI track1	CCL2_6
8	Aligner(KS)	13 sec. Hard contact.
9	Developer	65 sec.
10	Hard bake	20 min. 250C, ovn
11	RIE	MP_SOI2, 2,5 min.
12	Tencor	3-2,75µm step in center. 3,1-2,8µm at edged
13	RIE	OH_POLYA, 2x10 min.
14	Tencor	6,7µm step in center. 6,38µm at edged
15	RIE	MP_SOI2, 11 min.Thin film left. Newton rings.
16	RIE	MP_SOI2, 5 min.smaller rings.
17	Tencor	7,48µm step in center. 7,42µm at edged
18	RIE	MP_SOI2, 3 min.
19	RIE	MP_SOI2, 3 min.
20	RIE	MP_SOI2, 10 min. Still some left.
21	RIE	MP_SOI2, 4 min.
22	Acetone	20 min. With heat.
23	Anodically Bonded to P4	850V at 325C, Si wafer with metal used.

	Wafer	SEMI 5
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	HF 5%	15 sec.
4	RCA2	10 min.
5	Phospher Drive	WET1000, 10 min.
6	HMDS	30 min.
7	SSI track1	PR1_5
8	Aligner(KS)	10 sec. Hard contact.
9	Developer	55 sec.
10	HF 5%	4 min 30 sec. ??
11	Acetone	1/4 min.
12	HMDS	30 min.
13	Life time scan	avg: 10,33µs, min: 1,743µs, max:287,9µs, dev: 104%
14	SSI track1	PR1_5
15	Aligner(EVC)	8 sec. Mask no. 2.
16	Reversal bake	2 min. 120C contact heat.
17	Flood exposure(KS)	25 sec. Mask no. 3
18	Tencore	1,36µm step and 1,52µm step.

	Wafer	SEMI 6
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	HF 5%	15 sec.
4	RCA2	10 min.
5	Phospher Drive	DRY1000, 10 min. Cracks in all wafers!
6	Life time scan	avg: 10,06µs, min:0,123µs, max:81,74µs, dev:21,5%
7	SSI track1	PR1_5
8	Aligner(EVC)	8 sec. Mask no. 1.
9	Developer	55 sec.
10	HF 5%	4 min 30 sec.
11	Ion Implant	Boron, dose 2*10^11cm-^2
12	Acetone	1/5 min.
13	Tencor	1016 step. SIMS 1326Å burned resist.
14	HMDS	30 min.
15	SSI track1	PR1_5
16	Aligner(KS)	10 sec. Mask no. 2
17	Reversal bake	10 min. 120C contact heat.
18	Flood exposure(KS)	25 sec. Mask no. 3.
19	Tencor	1,36µm step and 1,52µm step.
20	Developer	55 sec.
21	Ion Implant	Boron, dose 5*10^15cm-^2 @ 150keV
22	Acetone	3 min coarse. 20 min. Fine. Still some left.
23	RIE	PR_STRIP, 10 min.

	Wafer	SEMI 7
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	HF 5%	15 sec.
4	RCA2	10 min.
5	Phospher Drive	DRY1000, 10 min. Cracks in all wafers!
6	Life time scan	avg: 10,2µs, min:0,219µs, max:26,75µs, dev:19,5%
7	HMDS	30 min.
8	SSI track1	PR1_5
9	Aligner(EVC)	9 sec. Hard contact, mask no. 1.
10	RIE	MP_SOI2, 2 min. 30 sec.
11	Ion Implant	Boron, dose: 2*10^11 @ 150keV
12	Tencor	2,84µm step in center. 2,82µm at edged

	Wafer	SEMI 8
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	HF 5%	15 sec.
4	RCA2	10 min.
5	Phospher Drive	DRY1000, 10 min. Cracks in all wafers!
6	Life time scan	avg: 9,232µs, min:0,208µs, max:132,3µs, dev:28,2%
7	SSI track1	PR1_5
8	Aligner(EVC)	8 sec. Mask no. 1.
9	Developer	55 sec.
10	HF 5%	4 min 30 sec.
11	Ion Implant	Boron, dose 2*10^11cm-^2
12	Acetone	1/5 min.
13	HMDS	30 min.
14	SSI track1	PR1_5
15	Aligner(KS)	10 sec. Mask no. 2
16	Developer	55 sec.
17	RIE	MP_SOI2, 2 min. 30 sec.
18	Acetone	25 min. Only 10% of the resist is removed.

	Wafer	SEMI 9
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	HF 5%	15 sec.
4	RCA2	10 min.
5	Phospher Drive	DRY1000, 10 min. Cracks in all wafers!
6	Life time scan	not done due to many flaws
7	HMDS	30 min.
8	HMDS	30 min.
9	SSI track 1	PR1_5
10	Aligner(KS)	10 sec. Hard Contact. Mask no. 1
11	Developer	60 sec. Old developer.
12	Optical Microscope	Resist test o.k.
13	RIE1	MP_SOI2. 2 min.
14	Optical Microscope	All oxide gone, AM good.
15	BHF m. vædemiddel	20 sec.
16	Ion Implant	BF2, 30keV, dose 2e11 cm^2
17	Acetone	1/15 min. Good result.
18	7-UP	H2O2 in first. 15 min
19	HMDS	30 min.
20	SSI track 1	PR1_5
21	Aligner(KS)	5 sec. HC. Mask no. 2
22	Reversal Bake	2 min. 120C contact heat.
23	Aligner(KS)	22 sec. HC. Mask no. 3
24	Developer	55 sec. (no entry in log)
25	Ion Implant	B, 30keV, dose 2e15 cm^2
26	Acetone	1/6 min
27	HMDS	30 min.
28	SSI track 1	PR1_5
29	Aligner(KS)	10 sec. Hard Contact. Mask no. 2
30	Developer	55 sec.
31	BHF m. vædemiddel	1min. 20 sec.
32	Acetone	1/20 min. Still some resist left.
33	RIE1	PR_strip 4 min. Newton rings
34	7-UP	10 min.
35	RCA1	10 min.
36	HF 5%	15 se.
37	RCA2	10 min.
38	Phospher Drive	3h oxidation, 20 min anneal. 1110Å(Calculated), DRY1000?
39	Optical Microscope	Resist on active areas!?
40	HMDS	30 min.
41	SSI track 1	PR1_5
42	Aligner(KS)	10 sec. HC. Mask no. 3
43	Developer	55 sec.
44	BHF m. vædemiddel	1 min. 40 sec.
45	HMDS	30 min. Forgot strip in acetone!
46	SSI track 1	PR1_5
47	Aligner(KS)	10 sec. HC. Mask no. 4
48	Developer	55 sec.
49	Alcatel	150/2000Å Ti/Al
50	Lift-off	10 min. Using new ace. Many particles, use other bench
51	HMDS	30 min.
52	SSI track 1	CCL2_6
53	Aligner(KS)	2x13 sec, due to error. HC. Mask no. 5.
54	Acetone	0/5 min.
55	HMDS	30 min.
56	SSI track 1	CCL2_6
57	Aligner(KS)	13 sec.
58	Developer	70 sec.
59	Resist Burn	20 min. 250C
60	BHF m. vædemiddel	1 min. 40 sec.

61	RIE1	OH_polya 10 min.
62	Tencor	4,68µm step center, 4,85 µm step side.
63	RIE1	5 min. + 2x1 min. +1,5 min. Total: 8,5 min.
64	Tencor	6µm step.
65	BHF m. vædemiddel	14 min.
66	Optical Microscope	The oxide seems to be gone, c.f. picture.
67	Acetone	0/10 min. Do not use liftoff bench - too many particles
68	Tencor	7,1µm step center, 6,5µm step side.
69	Anodically bonded to PT1	850V at 325C, Si protection wafer. AB did not work. Still resist!
70	RIE2	PR_strip x min.
71	Anodically bonded to PT1	850V at 350C. AB did not work!
72	Anodically bonded to PW5	850V at 350C.
72	Left the clean room	

	Wafer	**SEMI 10**
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	HF 5%	15 sec.
4	RCA2	10 min.
5	Phospher Drive	DRY1000, 10 min. Cracks in all wafers!
6	Life time scan	avg: 8,856µs, min:0,666µs, max:136,5µs, dev:31,3%
7	HMDS	30 min.
8	HMDS	30 min.
9	SSI track1	PR1_5
10	Aligner(EVC)	8 sec. Mask no. 1.
11	Developer	55 sec.
12	RIE	MP_SOI2, 2 min. 30 sec.
13	Acetone	1/20 min.Still remains. Due to RIE?
14	RIE	PR_STRIP, 5 min.
15	Tencor	593Å step. Which means that 400Å oxide is gone.
16	HMDS	30 min.
17	SSI track1	PR1_5
18	Aligner(EVC)	8 sec. Mask no. 2.
19	Flood exposure	25s mask no. 3.
20	Developer	55 sec.
21	Tencor	A narrow step in the middel of the plain.

	Wafer	**SEMI 11**
	Process	**Parameters and comments**
1	Wafer type	Si with 1000Å oxide, test of aligment mark in oxide
2	RCA1	10 min.
3	HF 5%	15 sec.
4	RCA2	10 min.
5	Phospher Drive	DRY1000, 10 min. Large crack in the oxide.
6	HMDS	30 min.

	Wafer	SOI1
	Process	**Parameters and comments**
0	Wafer type	SOI, n-type, {100}
1	RCA1	10 min.
2	HF 5%	15 sec.
3	RCA2	10 min.
4	Phospher Drive	WET1000. 10 min.
5	HMDS	30 min.
6	SSI track1	PR1_5
7	Aligner(KS)	10 sec. HC: Mask no. 1. Major flat downwards
8	Developer	55 sec.
9	Optical Microscope	good photolit. C.f. picture.
10	Tencor	1,5µm step.
11	RIE1	MP_SOI2. 2 min. 30 sec. Still oxide in centre.
12	RIE1	MP_SOI2. 30 sec. Still oxide in centre
13	Tencor	2,2µm step centre. 2,5µm step side.
14	HF 15%	25 sec.
15	BHF	20 sec.
16	Ion Implant	BF2, 30keV, dose 2e11 cm^2
17	Acetone	1/15 min. Good result.
18	7-UP	H2O2 in first. 15 min
19	HMDS	30 min.
20	SSI track 1	PR1_5
21	Aligner(KS)	5 sec. HC. Mask no. 2
22	Reversal Bake	2 min. 120C contact heat.
23	Aligner(KS)	22 sec. HC. Mask no. 3
24	Developer	55 sec. (no entry in log)
25	Ion Implant	B, 30keV, dose 2e15 cm^2
26	Acetone	1/6 min
27	HMDS	30 min.
28	SSI track 1	PR1_5
29	Aligner(KS)	10 sec. Hard Contact. Mask no. 2
30	Developer	55 sec.
31	BHF	1min. 20 sec.
32	Acetone	1/20 min. Still some resist left.
33	7-UP	10 min. Still resist left.
34	7-UP	10 min.
35	RCA1	10 min.
36	HF 5%	15 sec.
37	RCA2	10 min.
38	Phospher Drive	3h oxidation, 20 min anneal. 1110Å(Calculated), DRY1000?
39	Optical Microscope	Resist on active areas!?
40	BHF	2 min.
41	RCA1	10 min.
42	HF 5%	15 sec.
43	RCA2	10 min.
44	HF 5%	30 sec.
45	Phos. Predep	WET1000. Approx 7900Å-8800Å grown.
46	BHF	10+6 min.
47	RCA1	10 min.
48	HF 5%	15 sec.
49	RCA2	10 min.
50	HF 5%	30 sec.
51	Phos. Predep	DRY1000. 3h oxidation, 20 min. Anneal.
52	HMDS	30 min.
53	SSI track1	PR1_5
54	Aligner(KS)	10 sec. HC: Mask no. 1.
55	Developer	55 sec. Resist test fine. "Old" structures still visuable.
56	Ion Implant	BF2, 30keV, dose 1e12 cm^2
57	BHF	1 min. 40 sec. C.f. picture.
58	Acetone	1/10 min. Still resist left.
59	Acetone	0/3 min. Still resist left.

60	7-UP	10 min. 80C
61	HMDS	30 min.
62	SSI track 1	PR1_5
63	Aligner(KS)	4 sec. HC. Mask no. 2
64	Reversal Bake	2 min. 120C contact heat.
65	Aligner(KS)	25 sec. HC. Mask no. 3
66	Developer	60 sec.
67	Ion Implant	BF2, 30keV, dose 5e15 cm^2
68	Acetone	0/10 min.
69	7-UP	10 min. 80C
70	HMDS	30 min.
71	SSI track 1	PR1_5
72	Aligner(KS)	10 sec. HC. Mask no. 2
73	Developer	55 sec.
74	Resist burn	20 min. 250C
75	BHF	1 min. 40 sec.
76	Ion Implant	P, 100keV, dose 5e15 cm^2
77	RCA1	10 min.
78	HF 5%	15 sec.
79	RCA2	10 min.
80	Phospher Drive	DRY1000. 3h oxidation, 20 min. Anneal.
81	HMDS	30 min.
82	SSI track 1	PR1_5
83	Aligner(KS)	10 sec. HC. Mask no. 3
84	Developer	55 sec.
85	BHF	1 min. 40 sec.
86	Optical Microscope	Very small areas with oxide. C.f. picture
87	Acetone	1/6 min.
88	7-UP	10 min. 80C
89	HMDS	30 min.
90	SSI track 1	PR1_5
91	Aligner(KS)	10 sec. HC. Mask no. 4
92	Developer	60 sec.
93	Alcatel	150/2000Å Ti/Al
94	Lift-off	0/10 min.
95	Removing metal particles	Blue tape.
96	Acetone	6 min in glass beaker. Still some resist keft on the side.
97	HMDS	30 min.
98	SSI track 1	CCL2_6 (no log entry)
99	Aligner(KS)	10 sec. HC. Mask no. 5
100	Developer	70 sec.
101	Resist burn	20 min. 250C
102	BHF	1 min. 40 sec. (no log entry)
103	RIE1	OH_polya. 13 min. 30 sec.
104	RIE1	OH_polya. 2 min. 30 sec.
105	RIE1	OH_polya. 2 min. 30 sec. Still some left
106	Tencor	5µm step centre. 6µm step centre.
107	RIE1	OH_polya. 2 min.
108	RIE1	OH_polya. 3 min.
109	BHF	14 min.
110	Acetone	0/15 min. Still some resist left.
111	RIE1	PR_STRIP. 3 min.
112	Optical Microscope	Damage to conducting paths. C.f. picture.
113	Anodically bonded to PT1	800V at 350C. Protection wafer with 160Å oxide.
114	Saw	Si-cut:330µm Si left. Pyrex-cut: 300µm

	Wafer	SOI2
	Process	**Parameters and comments**
0	Wafer type	SOI, n-type, {100}
1	RCA1	10 min.
2	HF 5%	15 sec.
3	RCA2	10 min.
4	Phospher Drive	WET1000. 10 min.
5	HMDS	30 min.
6	SSI track1	PR1_5
7	Aligner(KS)	10 sec. HC: Mask no. 1. Major flat downwards
8	Developer	55 sec.
9	Optical Microscope	good photolit. C.f. picture.
10	RIE1	MP_SOI2. 3 min. Still oxide in centre.
11	Ion Implant	BF2, 30keV, dose 2e11 cm^2
12	Acetone	1/15 min. Good result.
13	7-UP	H2O2 in first. 15 min
14	HMDS	30 min.
15	SSI track 1	PR1_5
16	Aligner(KS)	5 sec. HC. Mask no. 2
17	Reversal Bake	2 min. 120C contact heat.
18	Aligner(KS)	22 sec. HC. Mask no. 3
19	Developer	55 sec. (no entry in log)
20	Ion Implant	B, 30keV, dose 2e15 cm^2
21	Acetone	1/6 min
22	HMDS	30 min.
23	SSI track 1	PR1_5
24	Aligner(KS)	10 sec. Hard Contact. Mask no. 2
25	Developer	55 sec.
26	BHF	1min. 20 sec.
27	Acetone	1/20 min. Still some resist left.
28	RIE1	PR_STRIP. 4 min. Newton rings
29	SEM	
30	7-UP	10 min.
31	RCA1	10 min.
32	HF 5%	15 sec.
33	RCA2	10 min.
34	Phospher Drive	3h oxidation, 20 min anneal. 1110Å(Calculated), DRY1000?
35	Optical Microscope	Good condition.
36	HMDS	30 min.
37	SSI track 1	PR1_5
38	Aligner(KS)	10 sec. Hard Contact. Mask no. 3
39	Developer	55 sec. Resist test o.k.
40	BHF	1min. 40 sec. Good AM.
41	HMDS	30 min. Forgot strip in acetone!
42	SSI track 1	PR1_5
43	Aligner(KS)	10 sec. HC. Mask no. 4
44	Developer	55 sec.
45	Alcatel	150/2000Å Ti/Al
46	Lift-off	15 min. Using new ace. Many particles, use other bench
47	Lift-off	10 min.
48	HMDS	30 min.
49	SSI track 1	CCL2_6
50	Aligner(KS)	13 sec. HC. Mask no. 5.
51	Developer	65 sec.
52	Resist burn	20 min. 250C
53	BHF	1 min. 40 sec.
54	RIE1	OH_polya 10 min.
55	Tencor	5,5µm step everywhere
56	RIE1	5 min.
57	Tencor	7,1µm step everywhere
58	BHF	2 min. 120C contact heat.
59	Tencor	7,18µm step center, 7,12µm step side.

60	RIE1	OH_polya 2 min. Some material have disapered
61	RIE1	OH_polya 30 sec. EPD still rising.
62	RIE1	OH_polya 30 sec. EPD still rising.
63	RIE1	OH_polya 30 sec. EPD ok.
64	Tencor	7,1µm step center, 7,3µm step side.
65	BHF	14 min.
66	Tencor	7,89µm step center, 7,47µm step side.
67	BHF	2 min.
68	Acetone	0/10 min.
69	Tencor	7,7µm everywhere.
70	Probe	144/200mV no light/light. 5,5M/170KOhm no light/light.
71	Acetone	separat bench + blue tape for cleaning.
72	SSI track2	PR6_2
73	Aligner(KS)	50 sec. HC. Mask no. 4.
74	Developer	3 min. 20 sec. Good photlit.
75	HF 5%	20 sec.
76	Alcatel	150/2000Å Ti/Al
77	Lift-off	10 min.

	Wafer	SOI3
	Process	**Parameters and comments**
0	Wafer type	SOI, n-type, {100}
1	RCA1	10 min.
2	HF 5%	15 sec.
3	RCA2	10 min.
4	Phospher Drive	WET1000. 10 min.
5	HMDS	30 min.
6	SSI track1	PR1_5
7	Aligner(KS)	10 sec. HC: Mask no. 1.
8	Developer	55 sec. Resist test fine.
9	BHF m. vædemiddel	1 min. 40 sec.
10	Ion Implant	BF2, 30keV, dose 1e12 cm^2
11	Acetone	1/10 min.
12	7-UP	10 min. 80C
13	HMDS	30 min.
14	SSI track 1	PR1_5
15	Aligner(KS)	5 sec. HC. Mask no. 2
16	Reversal Bake	2 min. 120C contact heat.
17	Aligner(KS)	22 sec. HC. Mask no. 3
18	Developer	60 sec.
19	Ion Implant	BF2, 30keV, dose 5e15 cm^2
20	Acetone	0/10 min.
21	7-UP	10 min. 80C
22	HMDS	30 min.
23	SSI track 1	PR1_5
24	Aligner(KS)	10 sec. HC. Mask no. 2
25	Developer	55 sec.
26	Resist burn	20 min. 250C
27	BHF m. vædemiddel	1 min. 40 sec.
28	Ion Implant	P, 100keV, dose 5e15 cm^2
29	RCA1	10 min.
30	HF 5%	15 sec.
31	RCA2	10 min.
32	Phospher Drive	DRY1000. 3h oxidation, 20 min. Anneal.
33	HMDS	30 min.
34	SSI track 1	PR1_5
35	Aligner(KS)	10 sec. HC. Mask no. 3
36	Developer	55 sec.
37	BHF m. vædemiddel	1 min. 40 sec.
38	Optical Microscope	Very small areas with oxide. C.f. picture
39	Acetone	1/6 min.
40	7-UP	10 min. 80C
41	HMDS	30 min.
42	SSI track 1	PR1_5
43	Aligner(KS)	10 sec. HC. Mask no. 4
44	Developer	60 sec.
45	Alcatel	150/2000Å Ti/Al
46	Lift-off	0/10 min.
47	Removing metal particles	Blue tape.
48	Acetone	6 min in glass beaker. Still some resist keft on the side.
49	HMDS	30 min.
50	SSI track 1	CCL2_6 (no log entry)

51	Aligner(KS)	10 sec. HC. Mask no. 5
52	Developer	70 sec.
53	Resist burn	20 min. 250C
54	BHF m. vædemiddel	1 min. 40 sec. (no log entry)
55	RIE1	OH_polya. 18 min. 30 sec.
56	Tencor	6,6µm everywhere.
57	BHF m. vædemiddel	14 min.
58	Acetone	0/15 min.
59	RIE1	PR_STRIP. 3 min. 30 sec. A few of the metal paths are damage!
60	Anodically bonded to SOI3	650V at 350C. Protection wafer with approx. 250Å oxide.
61	Saw	Si-cut:330µm Si left. Pyrex-cut: 300µm

	Wafer	**P1**
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	HMDS	30 min.
5	SSI track1	PR1_5
6	Aligner(EVC)	7 sec.
7	Reversal bake	20 min. Ovn
8	Developer	60 sec.
9	Alcatel	150/2000Å Cr/Au, Used a night to pump down.
10	Lift off	15 min. With sonic, try next time with heat. AM removed
11	Tencor	h=1843Å, width=581µm Xxhvilken bredde?XX
12	HMDS	30 min.
13	SSI track1	JTC4_2, This step was carried out 14 days before the next.
14	Aligner(KS)	18s only a quarter of the wafer is exposed. Best result.
15	Aligner(KS)	19s only a quarter of the wafer is exposed.
16	Aligner(KS)	19,5s only a quarter of the wafer is exposed.
17	Aligner(KS)	21s only a quarter of the wafer is exposed.
18	Developer	3 min. 20 sec.

	Wafer	**P2**
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	HMDS	30 min.
5	SSI track1	PR1_5
6	Aligner(EVC)	7 sec.
7	Reversal bake	20 min. Ovn
8	Flood exposure (KS)	25 sec.
9	Developer	60 sec.
10	HMDS	30 min.
11	Leybold	500Å Al
12	SSI track1	PR1_5
13	Aligner(EVC)	7 sec. Mask no.6
14	Reversal bake	2 min 90C contact heat.
15	Flood exposure (KS)	25 sec.
16	Developer	60 sec. Not all Al is gone.
17	Developer	45 sec. Wafer Broke.

	Wafer	P3
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	HMDS	30 min.
5	SSI track1	PR1_5
6	Aligner(EVC)	7 sec.
7	Reversal bake	20 min. Ovn
8	Flood exposure (KS)	25 sec.
9	Developer	60 sec.
10	HMDS	30 min.
11	Leybold	500Å Al
12	SSI track1	PR1_5
13	Aligner(EVC)	7 sec. Mask no.6
14	Reversal bake	2 min 90C contact heat.
15	Flood exposure (KS)	25 sec.
16	Developer	60 sec.
17	Developer	1 min. 45 sec. Up and down several times
18	Optical microscope	Digital sensor slit is gone.
19	Alcatel	150/2000Å Cr/Au. Used Ti to pump down.
20	Lift off	17 min.
21	Developer	1 min. 20 sec.Removal of Al.
22	HMDS	30 min.
23	SSI track1	JTC4_2
24	Aligner(KS)	22,5 sec.
25	Developer	XXX se cell 1164 side 7 book1
26	Plasma asher	2x1 min. 210 O2, 2min. 120 O2, N2
27	Aligner(KS)	3 sec.
28	Developer	30 sec. Unwanted resist is removed.
29	Poly etch	1 min. 20 sec. Error. Should have been hard baked.

	Wafer	P4
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	HMDS	30 min.
5	SSI track1	PR1_5, mask no. 6.
6	Aligner(EVC)	7 sec.
7	Reversal bake	20 min. Ovn
8	Flood exposure (KS)	25 sec.
9	Developer	60 sec.
10	The wafer must have been striped at this point due to the use of mask no. 6 again.	
11	HMDS	30 min.
12	Leybold	500Å Al
13	HMDS	30 min.
14	SSI track1	PR1_5, mask no. 6.
15	Aligner(EVC)	7 sec.
16	Reversal bake	2 min, 120C cantact heat.
17	Flood exposure (EVC)	25 sec.
18	Developer	1 min. 20 sec. Digsen gone, try shorter exp. Time.
19	Alcatel	150/2000Å Cr/Au, Used Ti to pump down.
20	Lift off	No lab entry!
21	HMDS	30 min.
22	SSI track1	JTC4_2, mask no. 7.
23	Aligner(KS)	22,5 sec.
24	Developer	1 min. 20 sec. Digsen gone, try shorter exp. Time.
25	Hard bake	5 min. 90C contact heat.
26	Poly etch	40 sec.
27	Tencor	4,8µm step.
28	Bluetape	
29	HF 40%	3 min. 18 sec.
30	Acetone	Removal of Bluetape. Still some glue on wafer.
31	Lift off	5 min. Not clean.
32	Lift off	5 min.
33	Poly etch	1 min.
34	Tencor	17,78 to 16,42µm step in the cavities.
35	Tencor	17,26 to 16,95 step in the cavities.
36	Tencor	9600Å to 9100Å step on slit side.
37	Tencor	9500Å to 9800Å step on slit side. How good is the Tencor?!
38	Tencor, Leybold test.	240Å Step.
39	Anodically bonded to SEMI4	

	Wafer	P5
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	HMDS	30 min.
5	SSI track1	PR1_5
6	Aligner(EVC)	7 sec.
7	Reversal bake	20 min. Ovn
8	Flood exposure (KS)	25 sec.
9	Developer	60 sec.
10	HMDS	30 min.
11	Leybold	500Å Al
12	HMDS	30 min.
13	SSI track1	PR1_5, mask no. 6.
14	Aligner(EVC)	7 sec.
15	Reversal bake	2 min, 120C cantact heat.
16	Flood exposure (EVC)	25 sec.
17	Developer	1 min. 20 sec. Digsen gone, try shorter exp. Time.
18	Alcatel	150/2000Å Cr/Au, Used Ti to pump down.
19	Lift off	No lab entry!
20	HMDS	30 min.
21	SSI track1	JTC4_2, mask no. 7.
22	Aligner(KS)	22,5 sec.
23	Developer	1 min. 20 sec. Digsen gone, try shorter exp. Time.
24	Hard bake	5 min. 90C contact heat.
25	Poly etch	40 sec.
26	Tencor	4,8µm step.
27	Bluetape	
28	HF 40 %	2 min. 15 sec.
29	Acetone	10 min.
30	HMDS	30 min.
31	Tencor	11,8µm step. Cavity side.
32	Tencor	4900Å step. Slit side.
33	SSI track1	PR1_5
34	Poly etch	50 sec.
35	Anodic Bonding	Bonded to SEMI 1

	Wafer	P6
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	HMDS	30 min.
5	SSI track1	PR1_5
6	Aligner(EVC)	7 sec.
7	Reversal bake	20 min. Ovn
8	Flood exposure (KS)	25 sec.
9	Developer	60 sec.
10	HMDS	30 min.
11	Leybold	500Å Al
12	SSI track1	PR1_5
13	Aligner(KS)	10 sec.
14	Reversal bake	2 min. 120C contact heat.
15	Flood exposure (KS)	25 sec.
16	Developer	55 sec.
17	Alcatel	150/2000Å Cr/Au. Possibly no Au left in tha Alcatel.
18	Lift off	17 min.
19	Developer	1 min. 30 sec. Removal of Al.
20	7-UP	10 min.
21	HMDS	30 min.
22	SSI track1	JTC4_2
23	Poly Etch	30 sec
24	Bake	12min at 120C
25	Blue tape	Au side
26	HF 40%	2min 20sec
27	Removal of Blue tape	
28	Acetone	
29	Poly Etch	2min
30	7-UP	10min
31	Anodically Bonded to SEMI3	850V at 320C

	Wafer	P7
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	HMDS	30 min.
5	SSI track1	PR1_5
6	Aligner(EVC)	7 sec.
7	Reversal bake	20 min. Ovn
8	Flood exposure (KS)	25 sec.
9	Developer	60 sec.
10	HMDS	30 min.
11	Leybold	500Å Al
12	SSI track1	PR1_5
13	Aligner(KS)	10 sec.
14	Reversal bake	2 min. 120C contact heat.
15	Flood exposure (KS)	25 sec.
16	Developer	55 sec.
17	Alcatel	150/2000Å Cr/Au. Possibly no Au left in tha Alcatel.
18	Lift off	17 min.
19	Developer	1 min. 30 sec. Removal of Al.
20	HMDS	30 min.
21	SSI track1	JTC4_2
22	Aligner(EVC)	16 sec.
23	Developer	3 min. 20 sec. Under exposed.
24	Developer	1 min. A bit better.
25	Acetone	1/10 min. 5 min. Is sufficient.
26	HMDS	30 min.
27	SSI track1	JTC4_2
28	Aligner(EVC)	16 sec. HC. Mask no. 7
29	Developer	3 min. 20 sec.
30	Developer	1 min.

	Wafer	P8
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	HMDS	30 min.
5	SSI track1	PR1_5
6	Aligner(EVC)	7 sec.
7	Reversal bake	20 min. Ovn
8	Flood exposure (KS)	25 sec.
9	Developer	60 sec.
10	HMDS	30 min.
11	Leybold	500Å Al
12		Scrathed

	Wafer	P9
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi, droped on the floor.
4	Poly etch	3 min. Still a thin film left.
5	7-UP	10 min. Still a thin film left.
6	Poly etch	20 min. Appear the be clean.
7	SSI track1	PR1_5
8	Aligner(EVC)	7 sec.
9	Reversal bake	20 min. Ovn
10	Flood exposure (KS)	25 sec.
11	Developer	60 sec.
12	HMDS	30 min.
13	Varian	100nm polySi..
14	HMDS	30 min.
15	SSI track1	JTC4_2
16	Aligner(KS) 1/6 of wafer exp.	20 sec. Resist test pattern.
17	Aligner(KS)	21 sec. No resist test pattern.
18	Aligner(KS)	22 sec. No resist test pattern.
19	Aligner(KS)	23 sec. Resist test pattern
20	Aligner(KS)	24 sec. No resist test pattern.
21	Aligner(KS)	25 sec. No resist test pattern.

	Wafer	P10
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi. Wafer broke.

	Wafer	P11
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi.
4	Leybold	100Å Al
5	HMDS	30 min.
6	SSI track1	PR1_5
7	Aligner (KS)	10 sec. Mask no. 6.
8	Reversal bake	2 min. 120C contact heat.
9	Flood exposure (KS)	25 sec.
10	Developer	55 sec.
11	Alcatel	150Å Cr

	Wafer	P12
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi.
4	Leybold	100Å Al
5	HMDS	30 min.
6	SSI track1	PR1_5
7	Aligner (KS)	11 sec. Mask no. 6.
8	Reversal bake	2 min. 120C contact heat.
9	Flood exposure (KS)	25 sec.
10	Developer	50 sec.
11	Alcatel	150Å Cr

	Wafer	P13
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	Leybold	100Å Al
5	HMDS	30 min.
6	HMDS	30 min.
7	SSI track1	PR1_5

	Wafer	P14
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	Leybold	100Å Al
5	HMDS	30 min.
6	HMDS	30 min.
7	SSI track1	PR1_5

	Wafer	P15
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi.
4	Leybold	100Å Al
5	HMDS	30 min.
6	HMDS	30 min.
7	SSI track1	PR1_5

	Wafer	P16
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi.
4	Leybold	100Å Al
5	HMDS	30 min.

	Wafer	P17
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	Leybold	100Å Al
5	HMDS	30 min.

	Wafer	P18
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	HMDS	30 min.
5	SSI track1	JTC4_2
6	Aligner (EVC)	18 sec. Mask no. 7
7	Developer	3 min 20 sec.
8	Developer	40 sec.

	Wafer	P19
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4	HMDS	30 min.
5	SSI track1	JTC4_2
6	Aligner (EVC)	19 sec. Mask no. 7
7	Developer	3 min 20 sec.
8	Developer	40 sec.

	Wafer	P20
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	7-UP	10 min.
3	Varian	0,1µm polySi
4		Lost in the Varian!

	Wafer	PS1
	Process	**Parameters and comments**
0	Wafer Type	Pyrex 500µm
1	Acetone	0/5 min.
2	HMDS	30 min.
3	SSI track1	PR1_5
4	Aligner(KS)	4 sec. HC. Mask no.6
5	Reversal bake	2 min. 120C
6	Aligner(KS)	25 sec.
7	Developer	55 sec
8	Alcatel	150/1700Å Cr/Au, machine error.
9	Lift-off	10 min.
10	Leybold	100/800Å Cr/Au
11	HMDS	30 min.
12	SSI track1	PR2_2
13	Aligner(KS)	13 sec. HC. Mask 7.
14	Developer	65 sec.
15	Au etch	20 sec.
16	Cr etch	3 min.
17	Resist burn	20 min. 250C
18	HF 40%	3 min. 10 sec.
19	Tencore	11,8 - 12µm step.
20	Acetone	0/10 min.
21	Tencore	11,3 - 9,7µm step.

	Wafer	PS2
	Process	**Parameters and comments**
0	Wafer Type	Pyrex 500µm
1	Acetone	0/5 min.
2	HMDS	30 min.
3	SSI track1	PR1_5
4	Aligner(KS)	4 sec. HC. Mask no.6
5	Reversal bake	2 min. 120C
6	Aligner(KS)	25 sec.
7	Developer	55 sec
8	Alcatel	150/2000Å Cr/Au.
9	Lift-off	10 min.
10	Leybold	100/800Å Cr/Au
11	HMDS	30 min.
12	SSI track1	PR2_2
13	Aligner(KS)	13 sec. HC. Mask 7. 5µm alignment error
14	Developer	65 sec.
15	Au etch	10 sec.
16	Cr etch	2 min.
17	Resist burn	20 min. 250C
18	HF 40%	3 min. 10 sec.
19	Tencore	11,4-11,8µm step.
20	Acetone	0/10 min.
21	Tencore	10,7 - 9,8µm step.

	Wafer	PS3
	Process	**Parameters and comments**
0	Wafer Type	Pyrex 500µm
1	Acetone	0/5 min.
2	HMDS	30 min.
3	SSI track1	PR1_5
4	Aligner(KS)	4 sec. HC. Mask no.6
5	Reversal bake	2 min. 120C
6	Aligner(KS)	25 sec.
7	Developer	55 sec
8	Alcatel	150/1500Å Cr/Au. Not anough Au in the machine.
9	Lift-off	10 min.
10	Leybold	100/800Å Cr/Au
11	HMDS	30 min.
12	SSI track1	PR2_2
13	Aligner(KS)	13 sec. HC. Mask 7. 5µm alignment error
14	Developer	65 sec.
15	Au etch	15 sec.
16	Cr etch	2 min. 30 sec.
17	Resist burn	20 min. 250C
18	HF 40%	2 min. 15 sec.
19	Tencore	9,9µm step.
20	HF 40%	1 min.
21	Acetone	0/10 min.
22	Tencore	12,5µm step.

	Wafer	PW1
	Process	**Parameters and comments**
0	Wafer type	Pyrex 500µm
1	Rinse	Water and soap
2	7-UP	10 min. 80C
3	Alcatel	150Å Cr. Not sufficient for good Photolit.
4	HMDS	30 min.
5	SSI track1	PR1_5
6	Aligner(KS)	4 sec. HC. Mask no. 6
7	Reversal bake	2 min. 120C. Contact heat.
8	Aligner(KS)	25 sec.
9	Developer	55 sec.
10	Alcatel	150/900Å Cr/Au, wrong deposition rate.
11	Lift-off	15 min.
12	HMDS	30 min.
13	SSI track1	PR2_2
14	Aligner(KS)	13 sec. HC. Mask no. 7
15	Developer	70 sec. Photolit o.k.
16	Cr etch	2 min. 120C. Contact heat.
17	Resist burn	20 min. 250C
18	HF 40%	2 min.
19	Tencore	8,6µm step centre, 8,8µm step side.
20	HF 40%	1 min. 20 sec.
21	Acetone	0/15 min. Resist not gone.
22	Acetone	0/15 min. Resist not gone.
23	Plasma Asher	5 min. Reci. 5, 1000W. Still resist left. No damage to Au
24	Plasma Asher	5 min. Reci. 5, 1000W. Still resist left. No damage to Au
25	Cr etch	>10 min. Not all Cr gone properly due to resist.
26	Plasma Asher	10 min. Reci. 5, 1000W.
27	7-UP	10 min. 80C

	Wafer	PW2
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	Rinse	Water and soap
3	7-UP	10 min. 80C
4	Alcatel	200Å Cr
5	HMDS	30 min.
6	SSI track1	PR1_5
7	Aligner(KS)	4 sec. HC. Mask no. 6
8	Reversal bake	2 min. 120C. Contact heat.
9	Aligner(KS)	25 sec.
10	Developer	55 sec.
11	Alcatel	150/1600Å Cr/Au, wrong deposition rate.
12	Lift-off	15 min.
13	HMDS	30 min.
14	SSI track1	PR2_2
15	Aligner(KS)	13 sec. HC. Mask no. 7
16	Developer	70 sec. Photolit o.k.
17	Cr etch	2 min. 120C. Contact heat.
18	Resist burn	20 min. 250C
19	Tencore	2,2µm step.
20	HF 40%	3 min. 20 sec.
21	Tencore	12,8µm step centre, 12,9µm step side.
22	Acetone	0/15 min. Resist not gone.
23	Acetone	0/15 min. Resist not gone.
24	Plasma Asher	15 min. Reci. 5, 1000W. Still resist left.
25	7-UP	10 min. 80C

	Wafer	PW3
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	Rinse	Water and soap
3	7-UP	10 min. 80C
4	Alcatel	200Å Cr
5	HMDS	30 min.
6	SSI track1	PR1_5
7	Aligner(KS)	4 sec. HC. Mask no. 6
8	Reversal bake	2 min. 120C. Contact heat.
9	Aligner(KS)	25 sec.
10	Developer	55 sec.
11	Alcatel	150/2000Å Cr/Au
12	Lift-off	15 min.
13	HMDS	30 min.
14	SSI track1	PR2_2
15	Aligner(KS)	13 sec. HC. Mask no. 7
16	Developer	70 sec. Photolit o.k.
17	Cr etch	2 min. 120C. Contact heat.
18	Resist burn	20 min. 250C
19	HF 40%	1 min. 20 sec.
20	Acetone	0/15 min. Resist not gone.
21	Acetone	0/15 min. Resist not gone.
22	Plasma Asher	15 min. Reci. 5, 1000W. Still resist left on 1/4 of wafer
23	Plasma Asher	5 min. Reci. 5, 1000W. Wafer rotated.
24	Plasma Asher	5 min. Reci. 5, 1000W. Wafer rotated.
25	Cr etch	2 min.
26	Optical microscope	Bonding interface not good. C.f. picture.
27	Cr etch	30 min.
28	Anodically bonded to BST3	650-700V at 350C.

	Wafer	PW4
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	Rinse	Water and soap
3	7-UP	10 min. 80C
4	Alcatel	200Å Cr
5	HMDS	30 min.
6	SSI track1	PR1_5
7	Aligner(KS)	4 sec. HC. Mask no. 6
8	Reversal bake	2 min. 120C. Contact heat.
9	Aligner(KS)	25 sec.
10	Developer	55 sec.
11	Alcatel	150/2000Å Cr/Au
12	Lift-off	15 min.
13	HMDS	30 min.
14	SSI track1	PR2_2
15	Aligner(KS)	13 sec. HC. Mask no. 7
16	Developer	70 sec. Photolit o.k.
17	Cr etch	2 min. 120C. Contact heat.
18	Resist burn	20 min. 250C
19	Droped on the table	
20	HF 40%	1 min. 20 sec.
21	Acetone	0/15 min. Resist not gone.
22	Acetone	0/15 min. Resist not gone.
23	Plasma Asher	15 min. Reci. 5, 1000W. Still resist left on 1/4 of wafer
24	Plasma Asher	5 min. Reci. 5, 1000W. Wafer rotated.
25	Plasma Asher	5 min. Reci. 5, 1000W. Wafer rotated.
26	Cr etch	2 min.
27	Optical microscope	Bonding interface not good. C.f. picture.
28	7-UP	10 min. 80C

	Wafer	PW5
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	Rinse	Water and soap
3	7-UP	10 min. 80C
4	Alcatel	200Å Cr
5	HMDS	30 min.
6	SSI track1	PR1_5
7	Aligner(KS)	4 sec. HC. Mask no. 6
8	Reversal bake	2 min. 120C. Contact heat.
9	Aligner(KS)	25 sec.
10	Developer	55 sec.
11	Alcatel	150/2000Å Cr/Au
12	Lift-off	15 min.
13	HMDS	30 min.
14	SSI track1	PR2_2
15	Aligner(KS)	13 sec. HC. Mask no. 7
16	Developer	70 sec. Photolit o.k.
17	Cr etch	2 min. 120C. Contact heat.
18	Resist burn	20 min. 250C
19	HF 40%	3 min. 20 sec.
20	Tencore	12,9µm step centre, 12,8µm step side.
21	Acetone	0/15 min. Resist not gone.
22	Acetone	0/15 min. Resist not gone.
23	Plasma Asher	15 min. Reci. 5, 1000W. Still resist left on 1/4 of wafer
24	Plasma Asher	5 min. Reci. 5, 1000W. Wafer rotated.
25	Plasma Asher	5 min. Reci. 5, 1000W. Wafer rotated.
26	Cr etch	2 min.
27	Optical microscope	Bonding interface not good. C.f. picture.
28	Cr etch	35 min.
29	HF 5%	20 sec.
30	7-UP	10 min. 80C
31	Anodically bonded to PW5	850V at 350C.
32	Left the Cleanroom	

	Wafer	PW6
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	Rinse	Water and soap
3	7-UP	10 min. 80C
4	Alcatel	200Å Cr. Flaw at edge.
5	HMDS	30 min.
6	SSI track1	PR1_5
7	Aligner(KS)	4 sec. HC. Mask no. 6
8	Reversal bake	2 min. 120C. Contact heat.
9	Aligner(KS)	25 sec.
10	Developer	55 sec.
11	Alcatel	150/2000Å Cr/Au
12	Lift-off	15 min.
13	HMDS	30 min.
14	SSI track1	PR1_5, resist on wrong side.
15	Acetone.	1/5 min.

	Wafer	PW7
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	Rinse	Water and soap
3	7-UP	16 min. 80C
4	Alcatel	1000Å Cr
5	HMDS	30 min.
6	SSI track2	PR6_2
7	Aligner(KS)	50 sec. HC. Mask no. 7
8	Developer	3 min. 20 sec.
9	Optical microscope	No significant different in photolit. Flaw in PR. Use 6 test wafers
10	Bake	20 min. 120C
11	Cr etch	10 min. 120mL RWF mix+80mL HNO3+1000mL H2O
12	Blue tape	
13	HF 40%	3 min. 20 sec.
14	Tencore	18,0µm step centre, 18,6µm step side.
15	Acetone	1/15 min
16	Cr etch	Untill Cr gone.
17	Tencore	12,3µm step centre, 12,4µm step side.
18	HMDS	30 min.
19	SSI track1	PR1_5
20	Aligner(KS)	4 sec. HC. Mask no. 6
21	Reversal bake	2 min. 120C
22	Aligner(KS)	25 sec.
23	Developer	55 sec
24	Alcatel	150/2000Å Cr/Au.
25	Lift-off	10 min.
26	7-UP	10 min. 80C

	Wafer	PW8
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	Rinse	Water and soap
3	7-UP	16 min. 80C
4	Alcatel	1000Å Cr
5	HMDS	30 min.
6	SSI track2	PR6_2
7	Aligner(KS)	53 sec. HC. Mask no. 7
8	Developer	3 min. 20 sec.
9	Optical microscope	No significant different in photolit. Flaw in PR. Use 6 test wafers
10	Bake	20 min. 120C
11	Cr etch	10 min. 120mL RWF mix+80mL HNO3+1000mL H2O
12	Blue tape	
13	Tencore	6,85µm step centre, 6,53µm step side.
14	HF 40%	3 min. 20 sec.
15	Acetone	1/15 min
16	Cr etch	Untill Cr gone.
17	Tencore	11,6µm step centre, 11,8µm step side.
18	HMDS	30 min.
19	SSI track1	PR1_5
20	Aligner(KS)	4 sec. HC. Mask no. 6
21	Reversal bake	2 min. 120C
22	Aligner(KS)	25 sec.
23	Developer	55 sec
24	Alcatel	150/2000Å Cr/Au.
25	Lift-off	10 min.
26	7-UP	10 min. 80C
27	Anodically bonded to SOI1	800V at 350C. Protection wafer with 160Å oxide.
28	Saw	Si-cut:330µm Si left. Pyrex-cut: 300µm

	Wafer	PW9
	Process	**Parameters and comments**
1	Wafer type	Pyrex 500µm
2	Rinse	Water and soap
3	7-UP	16 min. 80C
4	Alcatel	1000Å Cr
5	HMDS	30 min.
6	SSI track2	PR6_2
7	Aligner(KS)	55 sec. HC. Mask no. 7
8	Developer	3 min. 20 sec.
9	Optical microscope	No significant different in photolit.
10	Bake	20 min. 120C
11	Cr etch	10 min. 120mL RWF mix+80mL HNO3+1000mL H2O
12	Blue tape	
13	HF 40%	3 min. 20 sec.
14	Acetone	1/15 min
15	Cr etch	Untill Cr gone.
16	Tencore	11,6µm step centre, 11,6µm step side.
17	HMDS	30 min.
18	SSI track1	PR1_5
19	Aligner(KS)	4 sec. HC. Mask no. 6
20	Reversal bake	2 min. 120C
21	Aligner(KS)	25 sec.
22	Developer	55 sec
23	Alcatel	150/2000Å Cr/Au.
24	Lift-off	10 min.
25	7-UP	10 min. 80C
26	Anodically bonded to SOI3	650V at 350C. Protection wafer with approx. 250Å oxide.
27	Saw	Si-cut:330µm Si left. Pyrex-cut: 300µm

	Wafer	PT1
	Process	**Parameters and comments**
0	Wafer Type	Pyrex 500µm, Cr and PR on Cavity side.
1	Resist burn	20 min. 250C
2	HF 40%	3 min. 10 sec.
3	Tencore	17,6µm step centre, 16,9µm step side.
4	Acetone	0/10 min.
5	Acetone	0/10 min.
6	Aligner(KS)	25 sec.
7	Anodically bonded to SEMI9	850V at 325C, Si protection wafer. AB did not work. Still resist left on SEMI9
8	7-UP	20 min.
9	Anodically bonded to SEMI9	850V at 350C. AB did not work!

	Wafer	P?1
	Process	**Parameters and comments**
0	Wafer Type	Pyrex 500µm, polySi with JTC4_2 and Al on other side
1	Tencore	3,9µm step.
2	Bake	5 min. 90C
3	Poly Etch	40 sec.
4	HF 40%	3 min. 20 sec.
5	Acetone	0/5 min.
	Tencore	10,9µm step
6	7-UP	10 min. 80C
7	KOH	3 min 60C. Bonding interface is still "rough"

	Wafer	P?2
	Process	**Parameters and comments**
0	Wafer Type	Pyrex 500µm, polySi with JTC4_2 and Al on other side
1	Tencore	3,9µm step.
2	Bake	5 min. 90C
3	Poly Etch	40 sec.
4	HF 40%	3 min. 20 sec.
5	Acetone	0/5 min.
	Tencore	11,1µm step centre, 11,4µm step side.
6	7-UP	10 min. 80C
7	KOH	3 min 60C. Bonding interface is still "rough"

J

Papers Presented at Conferences

The list below describes articles that was presented during the project. The articles are found on the the subsequent pages.

16th Annual AIAA/USU Conference on Small Satellites
August 12-15, 2002. Utah State University, Logan, USA
Title: *Two-Axis MOEMS Sun Sensor for Pico Satellites* [13]
Authors: J.H. Hales and M. Pedersen

At this conference the authors participated in a student competition where a 4th place was obtained among 34 projects.

ESA's 4th Round Table on Micro/Nano Technologies for Space
May 20-22, 2003. ESA/ESTEC, Noordwijk, The Netherlands
Title: *Two-Axis MOEMS Sun Sensor and MEMS Electron Emitter Developed at MIC for DTUsat* [9]
Authors: R.W. Fléron, M. Pedersen, J.H. Hales, P.R. Bidstrup, and A. Torp

54th International Astronautical Congress
September 29 - October 3, 2003. Bremen, Germany
Title: *Linear Two-Axis MOEMS Sun Sensor and the Need for MEMS in Space* [35]
Authors: M. Pedersen, J.H. Hales, and R.W. Fléron

In this paper a discussion of why MEMS technology is a well suited technology for space applications is given. The reader is referred to appendix J to read about this.
ESA sponsored our participation, accommodation, and transport for this conference through their student outreach programme.